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Smart Spatial Light Modulator Research and Development

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Abstract

The objective of this research was to demonstrate "smart" spatial light modulators (S-SLM's) or smart pixels where electronic circuits are combined with optoelectronic components (i.e., lasers, modulators, and detectors). S-SLM's are the key components for high-speed, massively-parallel optical and optoelectronic interconnects and computing systems. The integration of mature electronic and optoelectronic components allows electronic processing elements to enhance their performance to levels not achievable by pure electronic implementation. During the duration of the project, we devoted our efforts in developing scalable fabrication technologies that allow integration of ferroelectric ceramic and semiconductors (Si, GaAs); technologies developed and implemented were direct-bonding and low-temperature flip-chip bonding. We also evaluated the performance potential of ferroelectric thin film multilayer-based light modulator and electrically tunable wavelength filter. The direct bonded technology that we developed is simpler and much more scalable than previous epitaxial lift-off (ELO) and bonding technologies. We have successfully combined direct bonding and flip-chip bonding technologies to realize functional smart pixel structures consisting of a direct-bonded high voltage Si driver circuit array and flip-chip bonded optically-addressable foundry logic chip.

Several spin-off technologies that warrant further investigation have also resulted from this research. These include: 1) physically flexible foundry-processed chip thinning and packaging technologies suitable for smart cards and aviation applications that require light-weight, shock-proof IC packaging and 2) high-efficiency, semi-transparent thin (1 μm thick) Si detector fabrication technology for passive sensor applications.

1. Developed Technologies

Our approach to realizing an S-SLM required the integration of arrays of high voltage driver circuits, processing elements, and modulators (bulk ferroelectric ceramic, III-V, or ferroelectric multilayer-based) in a monolithic geometry. Owing to the material and design incompatibilities among these components (e.g., difficulty associated with growing III-V or ferroelectric films on Si substrate or Si films on host substrates of modulating materials and the design complexity associated with integrating high voltage (≥ 20 V swing) driver circuit and low voltage logic circuit (5 V) on a single chip), truly monolithic integration of three component associated with an S-SLM is difficult. Thus, we decided that integration using grafting and bonding methods is better suited for combining the three associated components. To demonstrate our integration approach, we

fabricated several 2-dimensional S-SLM structures by grafting and direct-bonding a thin film containing driver circuit array onto a lead-lanthanum-zirconate-titanate (PLZT) substrate and flip-chip bonding to logic chips. We chose PLZT primarily because of its near 100% transparency compared to III-V MQW modulators that are inherently absorbing. A schematic illustration of an element in a complete S-SLM is illustrated in Fig. 1. For the integration, we developed two novel methods by which thin Si circuit films can be direct-bonded to any substrate and the pad metallurgy for a low temperature flip-chip bonding process. Direct bonding technique allows the realization of elements of high count and yield comparable to bulk foundry processes without sacrificing scalability for larger arrays. More logic (or smart) functionality for smart pixels is feasible drawing to the excellent quality of the thin film and the potential of flip-chip bonding for even larger electronic functionality.

In direct bonding technique, a free-standing thin film of the semiconductor material containing functional devices is obtained and subsequently bonded to the host substrate. The thin films with circuits can be generally obtained by epitaxial lift-off and substrate removal techniques. Lift-off of epitaxial device layers from their host semiconductor substrates and Van der Waals bonding to other substrates has been initiated for III-V compound semiconductors.

1.1 Direct Bonding of Thin Si Films onto PLZT for MOS Fabrication (DB1)

In the first direct-bonding approach (DB1), a high quality commercially available thin (2-4 μ m) Si film is bonded onto a transparent PLZT substrate using Van der Waals force and sequenced through a low temperature metal gate NMOS transistor processing steps to avoid thermal damage to the PLZT substrate. The details associated with this technology can be found in Appendix 1. Functional metal gate NMOS structures of various gate widths and lengths were fabricated onto the bonded Si films. These devices exhibited electrical performances that were comparable to that of similar devices fabricated on bulk Si. However, this approach may require the modification (e.g. low oxidation temperature) to the conventional MOS processing technology that may degrade the circuit performance.

1.2 Direct Bonding of Fabricated Circuits onto PLZT (DB2)

To resolve the scalability and circuit performance issues, we developed an alternative approach where a thin Si-on-insulator (SOI) film with prefabricated devices is grafted from its host Si wafer and bonded to a PLZT substrate (DB2). In DB2 technology, a commercially available SOI wafer with 0.6 - 1.0 μ m thick bulk-quality Si film on top of 1.0 μ m thick SiO₂ layer on a host Si substrate is sequenced through a conventional NMOS process. The host Si substrate is then removed by mechanical grinding to ~25 μ m thickness followed by SF₆ plasma etching. Here, the SiO₂ layer provides a self-termination point for the plasma etching step. The isolated circuit film is bonded to a PLZT substrate using a layer of epoxy (~1.0 μ m thick). Standard photolithography and metal deposition steps are then applied to electrically connect the circuit array to the PLZT

surface. The same technique can be applied to both foundry processed regular Si wafers and SOI wafers. A MOSIS chip has been also thinned down to 5 μm and bonded to a glass substrate. The Si substrate transparency at this thickness can be used as an etch control feature. The inherent oxide layers in SOI samples (ZMR, bond and etch back, SIMOX) provides an excellent self-stopping for the etch process thus allowing the bonding of thinner (less than 2 μm) films on larger scale. The electrical performance of the circuits is not affected by the grafting and bonding steps associated with DB2 (see Appendix 2). Any Si circuits can be bonded to host substrates using this approach. The advantage of imposing no limitation on the MOS processing parameters is self-evident. The bonded structure is demonstrated to withstand temperatures up to 300 C.

The advantage of DB2 approach is that most of the device fabrication steps are performed before the transfer and bonding of semiconductor layers. DB2 technology is highly scalable and does not impose any limitation on the MOS processing steps. This circumvents the stress build-up at the bonding interface that can result from high temperature processing steps and/or lattice mismatch. Large circuit areas ($> 25 \times 25 \text{ mm}$ -- limited only by initial sample size) has been grafted and bonded at better than 95% yield. Using DB2, we fabricated an 8×8 array of individually addressable Si/PLZT SLM shown in Fig. 2. This device consists of an array of 20 V swing driver circuits that is bonded to an array of 15 μm aperture PLZT modulator structures. In addition, we fabricated two (2) other SLM structures for a pattern-matching and network-switching Si/PLZT S-SLM demonstrations.

The advantages of direct bonding of Si to host substrates are:

- bulk quality silicon films can be combined with other substrates (e.g. GaAs, sapphire, PLZT, glass, metals etc) thus achieving unparalleled flexibility for Silicon-on-Insulator, optoelectronic, optical and micromechanical technologies.
- High complexity silicon circuits can be transferred to any substrate allowing any degree of smartness where it is needed.
- The resulting device structure is inherently a silicon-on-insulator structure therefore allows all the benefits of SOI such as high speeds (due to minimized capacitances) and higher breakdown.
- Substrate removal and bonding techniques are close to conventional silicon processing techniques, and can be extended to large substrates (e.g 100-150 mm diameter) with high yield and excellent manufacturability. Indeed, Kopin Corp. applies similar techniques to obtain high resolution liquid crystal head-up displays for virtual reality and or projection displays for HDTV applications.
- Resulting structures are very close to monolithic integration and therefore offers all the advantages of monolithic integration such as scalability, high density.
- The technique can be applied sequentially in horizontal and/or vertical dimension to obtain 2-D or 3-D integration of diverse semiconductor layers.

1.3 Low-Temperature Self-Aligning Flip-Chip Bonding

In order to add "smarts" (i.e. more logical functionality) to the Si/PLZT SLM's, we formulated a low-temperature flip-chip bonding technique for the Si/PLZT hybrid structures. As the epoxy used to direct-bond Si/PLZT SLM structure cannot tolerate more than 250°C for a prolonged period of time, it was necessary to develop a low temperature C4 reflow process. To accomplish this task, a ball-limiting pad metallurgy (BLM) that allows the use of near-eutectic Sn/Pb solder alloy was designed and fabricated. Here, Cr/Cr-Cu/Cu BLM layers are sputtered onto the connection pads on the direct-bonded Si/PLZT SLM's through a mask. Sn/Pb (60/40) alloy solder bumps (50 μm dia. and 25 μm thick) are then electroplated on top of the pads. Bonding pads on the foundry-processed logic chips are defined by electroless plating of Ni/Au (0.5 and 0.2 μm thick, respectively). The described metallurgy also can be utilized to achieve self-alignment of the bonding pads by exploiting the surface tension forces of the solder during the reflow. A designed experiment confirmed that initially misaligned chips can be self-aligned to better than 2 μm accuracy with the described pad geometry.

1.4 Ferroelectric Multilayer for SLM and WDM

To realize optical modulation using ferroelectric ceramic materials with low driving voltages, we explored the possibility of implementing ferroelectric multilayer deposition technology in collaboration with Rockwell International. Thin film deposition based technologies offer the advantage of scalable manufacturing. However, the modulation of a modulator based on a single thin ferroelectric layer is not high enough for system applications. Our calculations showed that both high reflector (HR) and Fabry-Perot (FP) filters consisting of ferroelectric multilayers can result in 0 to $\geq 90\%$ reflectance (with a corresponding contrast > 5000) change for 30 V voltage swing. As the ferroelectric film materials under consideration (i.e., PLZT, SBN, and PBN) do not absorb light for wavelengths above ~ 450 nm, such device can be expected to be much more efficient than MQW-based multilayer modulators. We developed a software code that can predict the performance of any arbitrary ferroelectric multilayer structures. A CCD array-based wide band spectrometer has been designed and constructed to characterize the spectral characteristics of ferroelectric multilayer-based devices. We have also initiated the concept of using similar thin film structures in electrically tunable filters for wavelength division multiplex applications.

Two ferroelectric multilayer samples were obtained from Rockwell International in a collaborative effort to evaluate their properties for the mentioned applications. These are 10 and 20 pair multilayer stacks of alternating PBN ($n=2.62$ $R_{eo}=1250 \times 10^{-12}$ m/V) and SBN ($n=2.34$ $R_{eo}=1350 \times 10^{-12}$ m/V) layers. The expected performance based on the measured properties is shown in Fig. 3. It shows that application of 40 V to 10 μm -spaced surface electrodes can should result in ~ 20 nm shift in the spectrum. The voltage requirement can be reduced further by implementing longitudinal transparent electrodes (ITO). We are continuing to pursue this project as it has evolved into a separate collaborative research effort with Rockwell International.

1.5 Direct-Bonding of III-V Devices onto Si Chip (DBIII-V)

As an alternative to using spatial light modulator arrays, we developed a reliable substrate removal technique to graft vertical-cavity surface-emitting laser (VCSEL) arrays onto Si chips based on DB2 technology described in Section 1.2. The integration of Si circuit with III-V devices can be obtained by either direct-bonding a Si circuit layer onto a III-V host substrate using DB2 or grafting a III-V device layer onto a Si chip. For the latter approach, epitaxial lift-off (ELO) process has attracted much effort in the past without yielding a commercially useful (simple and scalable) processing formula. With, minimal effort, we were able to extend the DB2 method to grafting and bonding III-V device layers (DBIII-V) much more reliably than with ELO process. The processing steps for DBIII-V are identical to that of DB2 with the exception of plasma source; here, CCl_2F_2 gas is used instead of SF_6 gas. Additional work need to be carried out to deposit and sinter ohmic contact metallurgy on grafted devices, but the process for grafting and handling wafer-size III-V device areas reliably have been developed and demonstrated.

2. Developed Smart SLM's

We have demonstrated complete smart SLM's by using developed direct-bonding and flip-chip-bonding methods for Si/PLZT integration. We utilized MOSIS foundry to fabricate optically-addressed pattern matching and network switching chips. These electronic processing chips were flip-chip bonded to corresponding Si/PLZT structures with direct bonded drivers and characterized.

2.1 Pattern-Matching S-SLM

A pattern matching S-SLM was fabricated primarily as a basis device to distribute large page-oriented memory blocks to an array of optically-addressed parallel processing elements. The "smart" part of this S-SLM is a foundry-processed chip that contains a 4×4 array of optically addressed local processing units that process and distribute appropriate portions of an incoming memory block to the corresponding processing elements. Each optically-addressed processing units conditions the input signal and compares it with pre-stored information (for pattern-matching) before transmitting the locally processed control signal to the corresponding output modulator in the flip-chip-bonded SLM. The SLM is fitted with a direct-bonded driver array that can be addressed electrically. A detailed photomicrograph in Fig. 4. shows the features of a fully assembled pattern-matching logic chip that is flip-chip bonded, using the described self-aligning C4 bonding technology, to a matching Si/PLZT SLM. When such S-SLM units are employed to distribute page-oriented memory blocks to an array of, say, 128×128 parallel processing elements with 64 bit channel width, we expect to be able to access 1 MB of information at MHz frame rates.

To demonstrate the described memory access concept, the pattern-matching chips were

utilized to construct a page-oriented database search system. The system divides a large memory page into blocks of four (4) sub-fields that is sequentially scanned by wavelength multiplexed holographic optical element (HOE). The scanned information is relayed to a memory interconnection processor (MIP) that consists of an array of memory distribution units; each memory distribution units consists of four (4) pattern-matching S-SLM's described previously to allow processing of 64 bit information database. In a database search cycle, the queries are first distributed to each memory distribution units in the MIP in parallel. Fields within each corresponding memory blocks are then searched sequentially by scanning the wavelength of the read-beam. Once the match is made, any information within the selected field can be read, conditioned, and relayed to the corresponding processing element in a parallel processor. The described system was utilized to store and read 64-bit airline flight information that were divided into airline identifier (16 bits), destination (24 bits), and departure and arrival times (24 bits) using a photorefractive crystal as memory media. Fig. 5 shows output summarizing the memory (bit) pattern of the searched field and the decoded result of this implementation. This type of S-SLM naturally lends itself to pattern-matching and other memory intensive applications that can utilize on-the-fly data pre-processing capability.

2.2 Twin Butterfly Network Switching S-SLM

A network switching S-SLM, shown in Fig. 6, was fabricated to demonstrate another class of application. This S-SLM was designed to function as a node in a twin butterfly interconnection network. The "smart" chip in this device consists of a processing logic circuit, four (4) input detectors to receive data from four input nodes from and four (4) output detectors to receive *clear-to-send* (CTS) signal from destination nodes. Each "smart" chip unit is connected to two (2) modulators on the flip-chip bonded Si/PLZT SLM. In each node, one modulator is dedicated to sending CTS signal back to the four input nodes while the other is used to send processed data output from the logic chip to four destination nodes. The fan-out of four (4) required by the twin-butterfly interconnection is performed by an external HOE. In a functional cycle, the logic circuit in a node receives a transmission request from a node in the input network stage. The node checks for the availability of buffer space and returns a CTS signal back to the input node. A data packet is then sent to the receiving node; the routing logic and switch sets the data into the proper output queue. The stored data is then relayed to the next stage through a repeated sequence. The oscilloscope traces in Fig. 7 shows TTL input to the pulsed optical source made incident on a node in a fabricated network-switching S-SLM and the processed optical signal output from a pixel in the S-SLM detected by an external PIN detector as illustrated by the diagram. Here, the information from four (4) inputs are multiplexed and sent to the output queue which controls the output modulator. The detected signal is the multiplexed signal from four input channels; thus, every fourth peak in the oscilloscope trace corresponds to the signal from one of the four input channels. This type of S-SLM can be utilized to realize ATM switching and FFT networks.

3. New Applications for Developed Technologies

The versatility of DB2 process allows the integration of thin Si devices onto virtually all types of surfaces; the substrate surfaces may be curved or flexible. In addition, semi-transparency of thin (1-2 μm thick) Si device layers may be utilized to obtain unique optoelectronic devices. In the following sections, we present the preliminary that examine two new applications for the technologies developed within this project. More details pertaining to these topics can be found in Appendix 3.

2.1 Semi-transparent Si Detector

During this project, we fabricated p-n⁺ junction detectors in bulk Si and commercially available SOI-Si wafers with two different Si layer thicknesses--1 μm SOI-Si from Kopin Corp. and 3 μm SOI-Si from SEH Corp. Thin detectors formed on SOI-Si are semi-transparent due to their thinness. A 1 μm thick Si detectors absorb only about 30% of the incident light at $\lambda=633$ nm. Thus, thin detector and amplifier circuit can be utilized as a passive sensor that can transmit 70% or more of the incident light signal. The effective quantum efficiencies (as measured) of 1 μm thick Si detectors are ~ 0.24 at $\lambda=633$ nm; this gives normalized quantum efficiency (compensated for finite absorption of ~ 0.30 at $\lambda=633$ nm for a 1 μm thick Si detector) of about .80. This is comparable to a bulk Si detector which has a quantum efficiency of about 0.82 at this wavelength. Measurements also indicated that a 3 μm thick detector performance is close to that of bulk detectors since it absorbs more than 70% of the incident light at $\lambda=633$ nm. Grafted and direct-bonded detectors also did not degrade in performance. The sensitivity is about 0.15 A/W and can be doubled by adding a metallic or dielectric mirror to the bottom of the detectors before bonding therefore reaching bulk values. The results indicate that these detectors can offer analog optical inputs suitable for control purposes and can also be operated at higher speeds due to the elimination of excessive capacitance and longer transit time of the carriers generated deep in the bulk. These results suggest that for S-SLM's, detector circuits may be integrated with the driver circuit in the direct-bonded thin Si layer to liberate more area on the foundry-processed chip for additional logic circuits.

2.2. Flexible Circuit Packaging

Owing to the thinness of initial SOI layer on Si substrate, which is typically ~ 2 μm thick, the isolated SOI layer is quite flexible after substrate removal. By inserting an additional flexible handling layer between the handling block and the SOI sample, the device layer can be bonded onto surfaces of almost any contour. We successfully transferred a 20 V driver array (used for S-SLM's) onto a flexible substrate to characterize the influence of bending on the electrical performance of the driver circuit. The same circuit was measured before and after wrapping the flexible circuit around a 1 cm dia. test tube as shown in Fig. 8. The electrical characterization

indicated that the applied amount of bending had no influence on the performance of the circuit when compared to the performance of an untransferred reference array in SOI-Si. Based on published data on fracture strength of Si, we confirmed that 1 μm thick Si films can be bent to less than 1 mm radius without fracturing. When thin circuit layers are packaged in flexible carriers (e.g., plastic cards or mylar films), packaged electronic or optoelectronic devices that are light, flexible, and shock-proof can be realized. Such devices may hold promise for both commercial (e.g., smart cards, cellular phones) and military (e.g., security, avionic electronics) applications.

Conclusion

During the duration of research, we developed several highly scalable hybridization technologies that were combined to fabricate several functional SLM and S-SLM devices. Direct-bonding methods for bonding wafer-sized Si device layers on other host substrates were developed. The metallurgy for a low temperature self-aligning flip-chip bonding process was identified and confirmed experimentally. These technologies were applied to fabricate an 8 x 8 individually addressable SLM consisting of Si driver circuits direct-bonded to a PLZT substrate and two (2) types of S-SLM structures consisting of an additional optically-addressed pattern matching or network-switching logic chip flip-chip bonded to a Si/PLZT SLM structure using the developed low-temperature C4 technology. The application potentials of ferroelectric multilayer films were analyzed and thin film deposition was demonstrated. The direct-bonding method was extended and tailored to graft III-V devices such as VCSEL's onto a Si chip. Novel extensions of the developed technologies such as semi-transparent Si detectors and flexible circuits were explored and demonstrated.

Appendix (Publications)

- [1] J.H. Wang, M.S. Jin, V.Ozguz, and S.H. Lee, "N-channel metal-oxide-semiconductor transistors fabricated in a silicon film bonded onto sapphire," *Appl. Phys. Lett.* Vol.64, 724-726, (1994).
- [2] M. S. Jin, J. H. Wang, V. Ozguz and S. H. Lee, "Monolithic integration of Si driver circuit onto PLZT substrates for smart spatial light modulator fabrication," *Appl Opt.*, Vol.33, 2842-2849, (1994).
- [3] M. S. Jin, J. H. Wang, D. T. Lu, V. Ozguz, and S. H. Lee, "Direct-bonding and Flip-chip Bonding Technologies Applied to Si/PLZT Spatial Light Modulator Fabrication," Proceedings of the Annual Motorola ECTC Conference (Las Vegas, NV), May 1995.

Conference Presentations

- [1] M.S. Jin, J.H. Wang, V. H. Ozguz, and S.H. Lee, "Bonding of Si thin films to PLZT Substrates for Smart Spatial Light Modulator Applications" presented at the OSA Topical Meeting on Spatial Light Modulator, Paper No. STuB2, Palm Springs, CA, March 1993.
- [2] M. S. Jin, J. H. Wang, S. Patra, V. Ozguz, and S. H. Lee, "Lead Lanthanum Zirconate Titanate (PLZT) Smart Spatial Light Modulator (S-SLM) Consisting of Direct-Bonded Driver Circuit and Flip-Chip Bonded Processor," presented at 1994 IEEE Conference on Smart Pixel and Applications, Lake Tahoe, CA, 4-8, July 1994.
- [3] M. S. Jin, J. H. Wang, D. T. Lu, V. Ozguz, and S. H. Lee, "Direct-bonding and Flip-chip Bonding Technologies Applied to Si/PLZT Spatial Light Modulator Fabrication," to be presented at Annual Motorola ECTC Conference (Las Vegas, NV), May 1995.

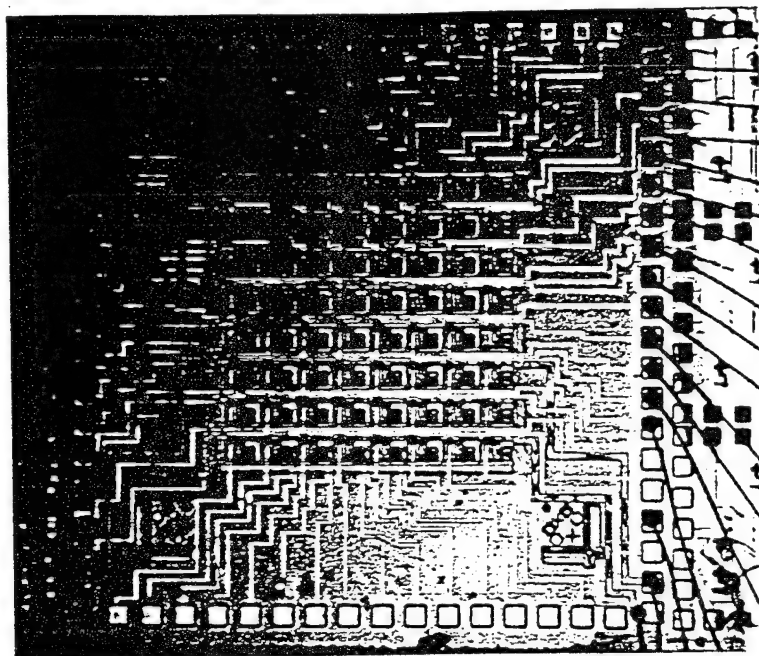


Fig. 2. A photomicrograph of an 8 x 8 Si/PLZT SLM with thin Si film (2 μ m thick) driver circuit array direct-bonded to a PLZT substrate.

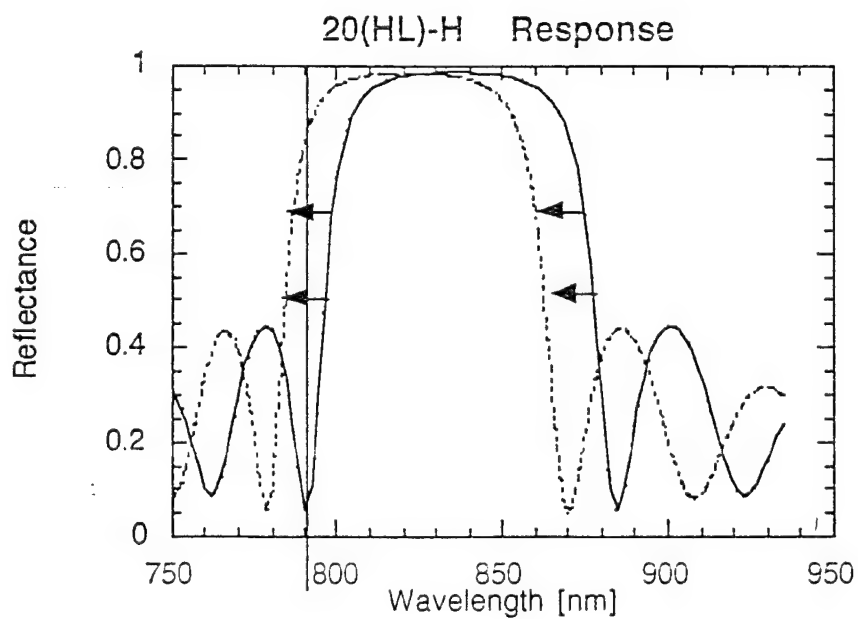


Fig. 3. Reflectance spectra of a 20 pair PBN/SBN ferroelectric high reflector stack with 10 μ m spaced surface electrodes at 0 V (solid) and 40 V (dashed).

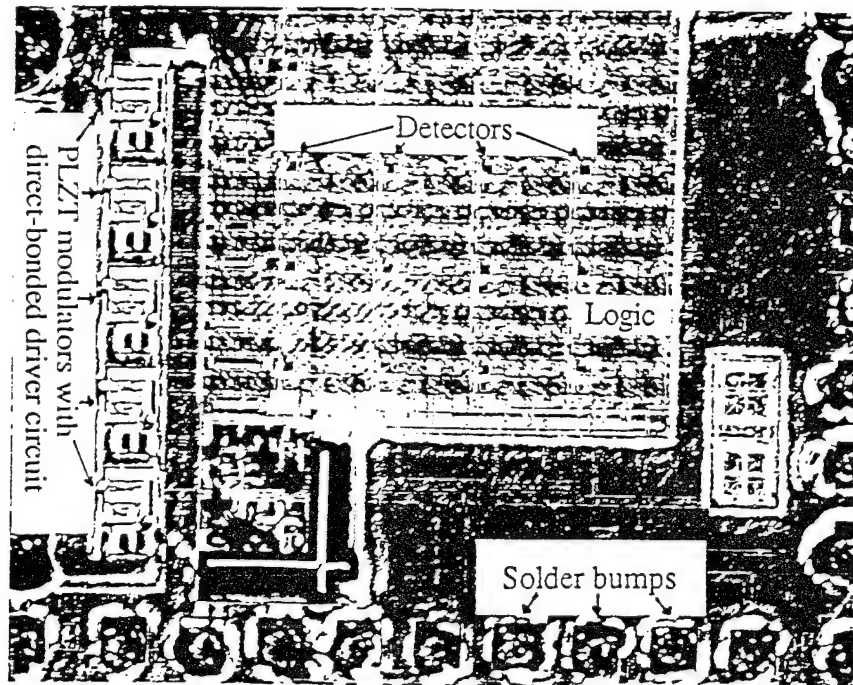


Fig. 4. A photomicrograph of a fully assembled pattern matching S-SLM that consists of a direct-bonded Si/PLZT SLM that is addressed by a flip-chip bonded optically addressable logic chip.

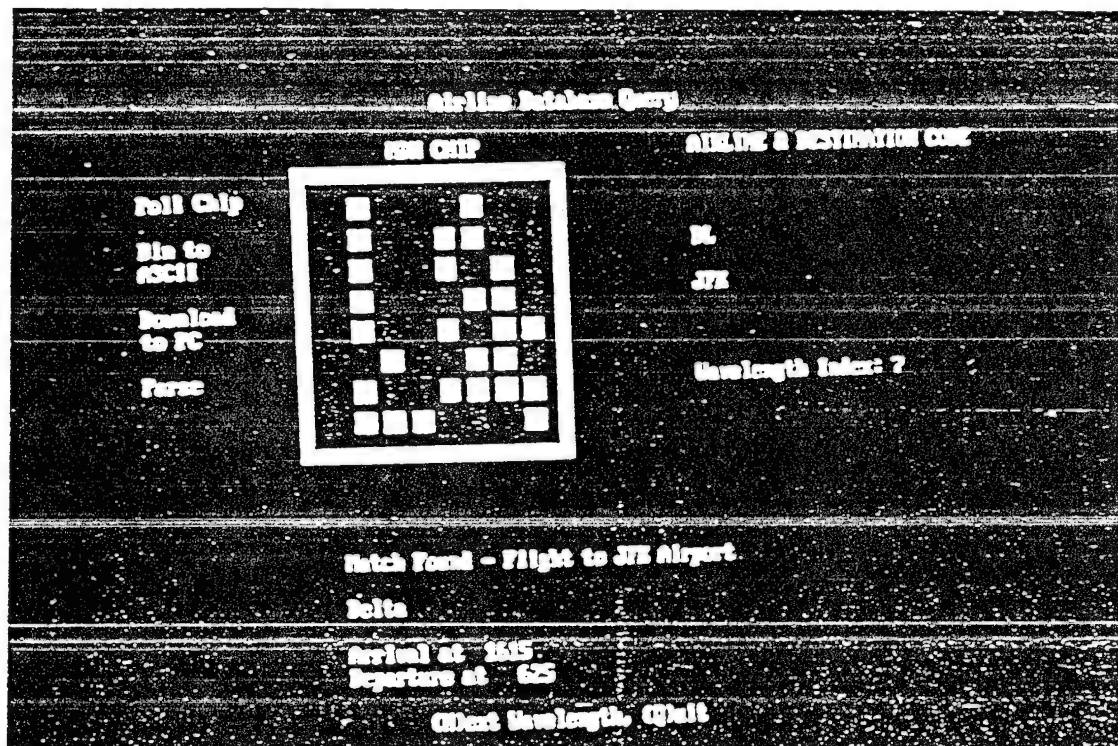


Fig. 5. Software controlled data search output on PC. Memory distribution S-SLM's are implemented to search and match in parallel the memory blocks in a page memory stored on a photorefractive crystal. The pattern represents the actual physical layout of the bit memory in a matched field within the searched memory block.

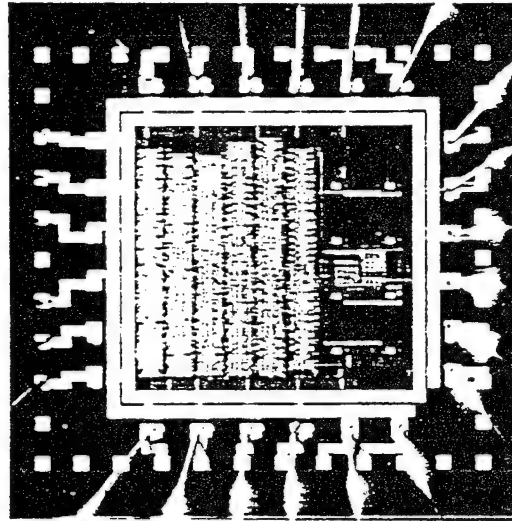


Fig. 6. A photomicrograph of a MOSIS processed optically addressable logic chip for network switching S-SLM.

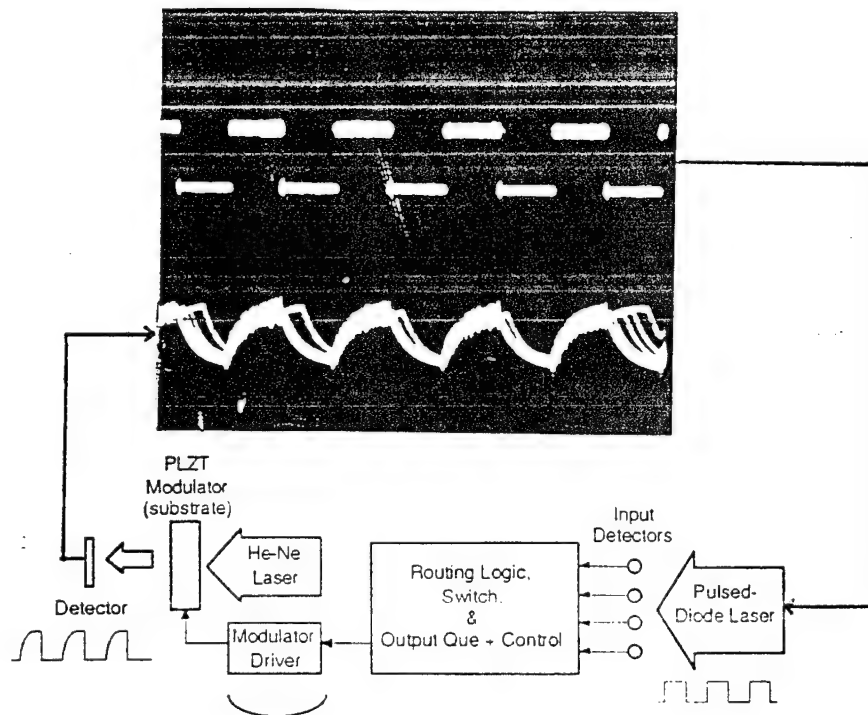


Fig. 7. Oscilloscope trace of detected signal at the output of SLM pixel driven by an optically-addressed network-switching logic chip. Schematic diagram illustrates the full functionality of the network-switching S-SLM structure.

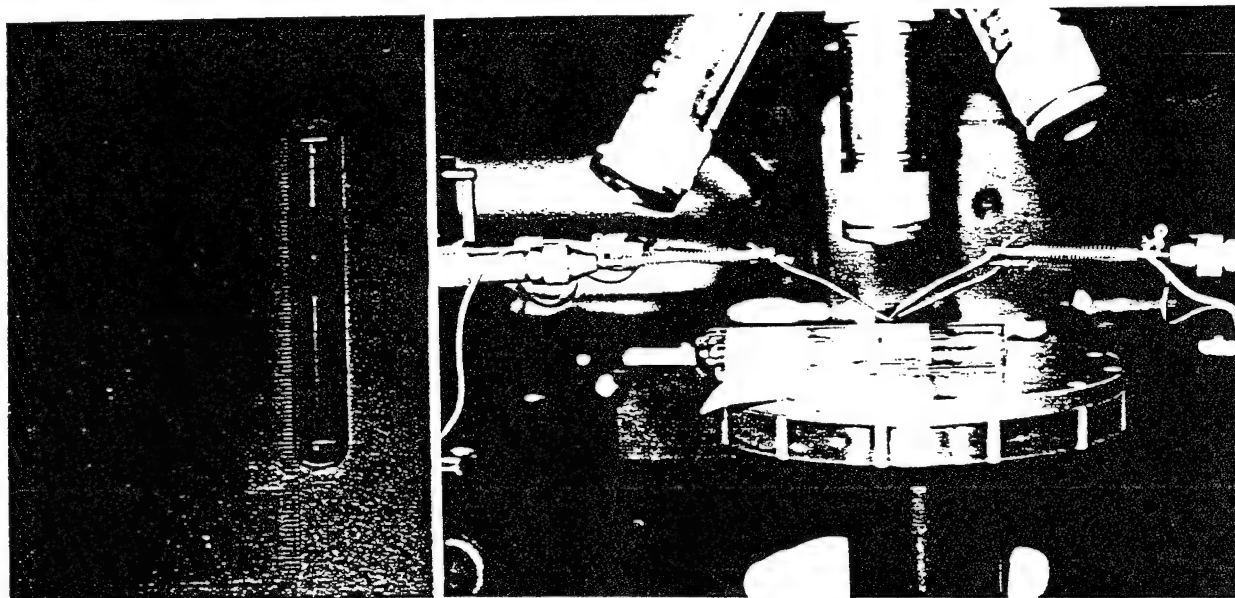


Fig. 8. Photomicrographs of a flexible circuit wrapped around a 0.5 cm radius test tube in a characterization set-up.

N-channel metal-oxide-semiconductor transistors fabricated in a silicon film bonded onto sapphire

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N-channel metal-oxide-semiconductor transistors were fabricated in silicon films that were bonded onto sapphire substrates. The bonded silicon films can withstand high processing temperatures (850 °C). The electrical performance of the resulting devices is comparable to that of devices fabricated in bulk silicon wafers. This technology can be applied to silicon-on-insulator device development and for integrated optoelectronic device research.

Silicon on insulator (SOI) technologies are showing promise for ultra large scale integrated circuits (ULSI) and radiation hardening devices applications.¹ Currently, SOI materials can be categorized into two groups in which (i) a silicon device layer is obtained on a silicon substrate [e.g., separation by implanted oxygen (SIMOX), zone-melting-recrystallization (ZMR), and wafer bond and etch back]; or (ii) a silicon device layer is obtained on sapphire (SOS) by gas phase epitaxy. Both groups have a common feature: the silicon device layer is obtained by some high-temperature (>1000 °C) processing steps (e.g., recrystallization, annealing, bonding, epitaxy). The use of high temperature eliminates the possibility of using substrates that cannot withstand high temperature such as lead lanthanum zirconate titanate (PLZT); thus restricting the use of such techniques in optoelectronics.²

Lifting off the epitaxial layers from their bulk semiconductor substrates and Van der Waals bonding (grafting) to other substrates emerged as a new technique during the last four years.³ This bonding technique was originally developed to graft III-V compound semiconductors (i.e., GaAs and InP) onto various host substrates, such as glass, sapphire, and LiNbO₃. Here, most of the device fabrication processes are completed before the transfer and bonding of semiconductor layers to avoid stress on the bonding interface that may result from high-temperature processing steps.

We were successful in developing a Van der Waals bonding technique for obtaining high-quality single-crystalline silicon film on a sapphire substrate. N-channel metal-oxide-semiconductor (NMOS) transistors were fabricated in these silicon films after the bonding by using high temperature steps (up to 850 °C) without damaging the bond. This will enable the realization of electronic circuits on a variety of substrates with bulk quality silicon film. We report here the preliminary device characterization results.

For the experiment, a 2-in.-diam, 4- μ m-thick, *p*-type, <100> oriented, 8–10 Ω cm resistivity single-crystalline silicon film (supplied by Virginia Semiconductor Inc.) was used. This film was first cleaned with trichloroethylene (at 80 °C) and then with acetone (at 60 °C), followed by base and acid solution (RCA) cleaning at 85 °C. During these cleaning processes, the thin film was left unsupported in the solutions, and agitating gas bubbles that could damage the thin silicon film were prevented from forming in the solutions. The

silicon film surface became hydrophilic by the end of the cleaning steps. After a few minutes of rinsing in de-ionized water, the wet film was transferred onto the surface of a <1102> oriented sapphire wafer at room temperature. The sapphire wafer had both sides polished to optical flatness and was pretreated with 10% HF. The film was moved gently until it was properly positioned on the substrate. There was no need to align the silicon and sapphire lattice orientations⁴ since Van der Waals bonding depends only on the force between the molecules on the bonding surfaces. The excess water was then blotted up by using pressure less than 1.5×10^4 dyn/mm² (Ref. 5) until the interference fringes disappeared and a uniform dark color emerged in the silicon film region when observed from the back side of sapphire. Unlike in the lift-off and bonding of GaAs epitaxial layers, we did not apply Apiezon wax on the silicon film for support. This resulted in easier post-bonding cleaning. We found that unsupported silicon film (4 μ m thick) was rugged enough to withstand moderate handling. After the pressure was released, these bonded silicon films were placed in a clean container at room temperature. The water remaining between the film and the substrate evaporated within 24 hs.

Processing sequence for fabricating metal gate NMOS transistors in silicon layer bonded on sapphire is illustrated in Fig. 1. The sequence can be easily modified for poly-gate NMOS fabrication. A test structure consisting of transistors with 5, 10, and 15 μ m of gate lengths and 10, 20, and 30 μ m of gate widths was fabricated. First, the silicon film was dry etched by a collimated argon ion beam (RIBE). The etching angle was 45°. After the ion milling of silicon outside the photoresist mask, isolated silicon islands with a trapezoid cross section remained. The photoresist remaining after RIBE was removed by oxygen plasma etching. Subsequently, 1.6–1.7 μ m thick SiO₂ layer was deposited by plasma-enhanced chemical vapor deposition (PECVD). A masking step was used to chemically etch away this layer from the top surfaces of silicon islands. The rest of the deposited SiO₂ layer was protected during the etch to remain on the substrate and on the side walls to provide passivation as well as additional clamping to support the silicon islands [Fig. 1(a)]. Another 400 nm of PECVD SiO₂ was deposited as a mask layer, and drain and source regions were opened

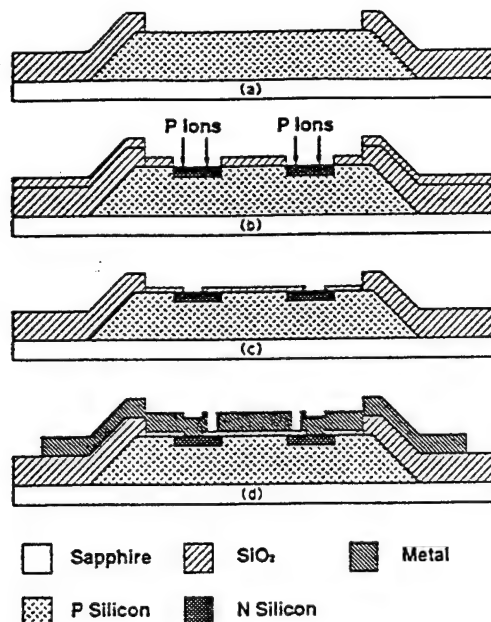


FIG. 1. Processing sequence of the NMOS device fabrication in thin silicon film directly bonded onto sapphire substrate.

on this layer for ion implantation [Fig. 1(b)]. Phosphorus ions were then implanted at a dosage of $6 \times 10^{14}/\text{cm}^2$ and an energy of 50 keV. Afterwards, the SiO_2 mask layer was removed from the gate regions. A gate oxide layer was grown by applying pyrogenic oxidation at 850 °C for 1 h, this step also served to activate the implanted phosphorus ions. The temperature was ramped at less than 10 °C/min in order to minimize the stress between silicon, SiO_2 , and sapphire. Contact windows were etched in the oxide [Fig. 1(c)], and a 1.2- μm -thick layer of aluminum was deposited for metallization. The aluminum layer was patterned [Fig. 1(d)] and then sintered at 450 °C in forming gas to reduce fixed interface states.

After completion of the processing steps, very few cracks were observed in bonded thin silicon islands under the microscope. A photomicrograph of the finished device is shown in Fig. 2. Our observation confirmed that the bonding

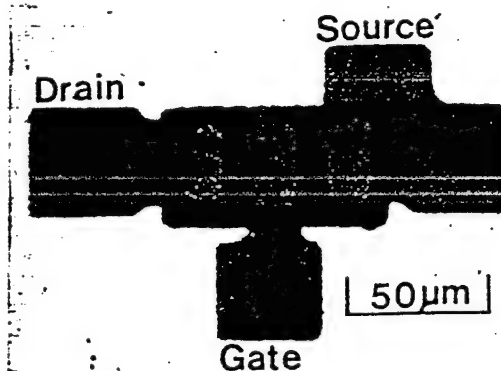


FIG. 2. Photomicrograph of NMOS transistor fabricated in a thin silicon film directly bonded onto a sapphire substrate.

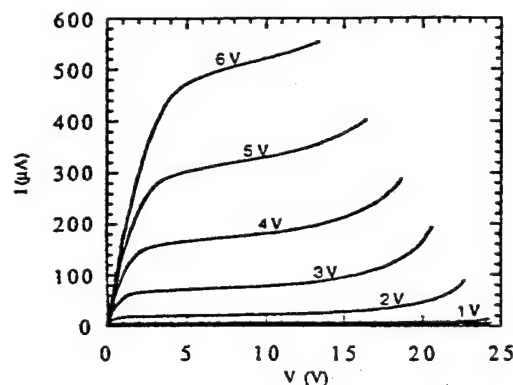


FIG. 3. Typical I - V curve of NMOS transistor fabricated in directly bonded silicon film with 10- μm gate length and 20- μm gate width.

interface and the bonded silicon film remained structurally stable under the above-mentioned process conditions. The threshold voltages of NMOS transistors were narrowly distributed between 1.0 and 1.2 V and did not differ for 5-, 10-, and 15- μm gate lengths. The source-drain breakdown showed a sharp avalanche behavior at about 25 V. This breakdown is less than that of p - n junction fabricated in an 8- Ω cm resistivity substrate. The difference is expected to result from parasitic bipolar transistor effects, since the minority carrier lifetime of the bonded thin silicon film is rather long.⁶ For most of these devices, the leakage currents were around 20 pA for 1 μm of gate width after the forming gas sintering. The leakage current may be reduced by improving the process environment and anneal process. A typical I - V curve of a 10- μm gate length and 20- μm gate width transistor is shown in Fig. 3. Based on this curve, the channel electron mobility was calculated to be 470 $\text{cm}^2/\text{V s}$. This value is lower but close to that of NMOS devices fabricated in bulk silicon wafer.

In summary, we have demonstrated the operation of first MOS devices fabricated in thin silicon film Van der Waals bonded onto a sapphire substrate. Bonded thin silicon islands, clamped by PECVD SiO_2 film, can withstand moderate (850 °C) processing temperatures. The electrical performance of the resulting devices is comparable to that of devices fabricated in bulk silicon wafers. The amount of leakage current of these devices suggested that the interface state density between silicon and sapphire substrate is low enough to ensure acceptable device performance; it is comparable to that between silicon and SiO_2 in conventional SOI wafer. Similar to silicon on sapphire prepared by direct bonding and back etching,⁴ this is a new technique to prepare SOS wafer with bulk quality silicon film. It can extend the application of SOS wafer to minority carrier devices, such as charge couple devices and bipolar circuits. This technology holds promise for Van der Waals bonding thin silicon films onto other electro-optic materials or transparent substrates, such as quartz, LiNbO_3 , and PLZT. Device processing after the bonding of silicon film permits batch fabrication of de-

vices for circuits and ensures their alignment to existing components or circuits with photolithographic accuracy. Although the description of our technology emphasizes the integration of silicon circuits with optical components, it can also be extended to the fabrication of stacked three-dimensional circuits.

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Monolithic integration of a silicon driver circuit onto a lead lanthanum zirconate titanate substrate for smart spatial light modulator fabrication

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The monolithic integration of *N*-channel metal-oxide-semiconductor (NMOS) driver circuits in silicon thin films onto a lead lanthanum zirconate titanate (PLZT) substrate is reported. Two integration methods are compared. Both methods result in NMOS transistors that exhibit electrical properties that are close to those of transistors fabricated in bulk silicon. The characteristics of PLZT modulators driven by thin-film transistors are also similar to those of bulk PLZT modulators. These techniques promise new spatial light modulators of high complexity and performance that good-quality silicon and bulk PLZT can offer.

1. Introduction

The realization of smart spatial light modulators (S-SLM's) by the combination of electronic processing materials (e.g., Si and GaAs) and light modulation materials (e.g., ferroelectric ceramics or liquid crystals and III-V semiconductors) is essential for many tasks associated with the development of optoelectronic and optical computing. Recently, the possibility of fabricating sophisticated S-SLM's based on ferroelectric liquid-crystal and Si circuits has been demonstrated, but the operating speeds of these S-SLM's are relatively slow.¹⁻³ Exceptionally high modulation speed multiple-quantum-well-based S-SLM's, such as a field-effect transistor self-electro-optic-effect device (FET-SEED), have also been demonstrated, although the inherent absorption limits the light throughput and may cause a heat dissipation problem.⁴ To find a better compromise between speed and light throughput, we have been studying S-SLM's that combine the mature Si electronic technology and lead lanthanum zirconate titanate (PLZT) (a transparent, ferroelectric ceramic) modulators. Their operating speeds are expected to be between those of the Si/ferroelectric liquid-crystal and the

FET-SEED devices; the PLZT modulators do not absorb light.

In the past, other approaches for combining Si with PLZT have been studied.^{5,6} However, in the approach in which a PLZT film is deposited on the windows of Si on sapphire, the light modulator is not effective because the maximum PLZT film thickness obtainable through deposition is far too thin. In the approach in which amorphous Si is deposited on bulk PLZT and then recrystallized, the quality of recrystallized Si is not high enough to implement large numbers of transistors and efficient light detectors.⁷ In the flip-chip bonding approach, in which bulk quality Si is combined with bulk PLZT, there is a voltage compatibility problem that causes difficulties for inclusion of the modulator driver circuit (requiring 20–50 V) in the Si wafer that contains the logic circuits (operating at 5 V).

To overcome these limitations, we studied methods to bond Si-based driver circuits directly onto the bulk PLZT substrate. Sophisticated logic circuits would still be implemented in the bulk, foundry-processed Si wafers with excellent lifetime and minimum defect densities; this wafer will be flip-chip bonded to the Si film that contains the driver circuit array that is directly bonded on bulk PLZT. The top view of a Si/PLZT S-SLM and the cross section of one of its unit cells are illustrated in Fig. 1.

We investigated two direct-bonding (DB) techniques for combining thin silicon films with bulk PLZT:

DB1: Bonding of commercially available 2–4- μm -

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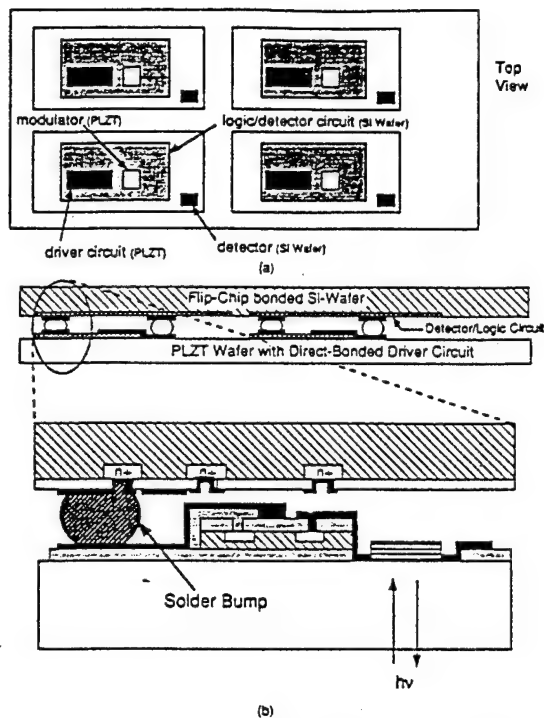


Fig. 1. (a) Top view of a Si/PLZT S-SLM with four cells in a 2×2 array. (b) Cross section of one unit cell of a Si/PLZT S-SLM. A thin Si film with a driver circuit is bonded directly to bulk PLZT and flip-chip bonded to a Si wafer with detector and logic circuits.

thick Si films onto PLZT, followed by fabrication of metal-oxide-semiconductor (MOS) devices. This method utilizes thicker Si films ($2\text{--}4\text{ }\mu\text{m}$ thick) that will permit the realization of more efficient Si detectors for optical addressing.

DB2: Fabrication of MOS devices in Si-on-insulator (SOI) silicon wafers, followed by lift-off of thin silicon film-containing devices and bonding to bulk PLZT. This approach permits the implementation of conventional Si device processing steps.

After the bonding was completed, modulator windows were defined through the bonding layers, and a layer of metal was deposited to make an electrical connection between the transistors and the PLZT substrate.

Lift-off of epitaxial device layers from their host semiconductor substrates followed by van der Waals bonding to other substrates has become a well-established technology for III-V compound semiconductors.⁸⁻¹⁰ There, most of the device fabrication processes are performed before the transfer and bonding of semiconductor layers. This circumvents the stress buildup at the bonding interface that can result from high-temperature processing steps. For Si and PLZT systems, this technology had to be modified as described above for DB1 and DB2 methods in order to accommodate the change in materials involved. Both methods proved to be fruitful, and as a consequence, we were allowed to choose between the two by considering manufacturing issues such as

desired device, yield, scalability, and required processing time. Here we present the experimental outline and the outcome of both bonding methods before emphasizing a particular method, as they are both new processing technologies that may be explored for various optoelectronic applications.

2. Outline of Experiments

For the first method (DB1), we developed a processing technique to bond a Si film to a PLZT substrate and fabricate *N*-channel MOS (NMOS) devices through a series of low-temperature MOS processing steps that prevent thermal damage to the PLZT substrate. For this purpose, a clean 2-in.- (5.08-cm-) diameter, $4\text{-}\mu\text{m}$ -thick silicon film from Virginia Semiconductor Inc. was van der Waals-bonded to a PLZT substrate with a 20-nm-thick Al_2O_3 buffer layer (see Fig. 2) and sequenced through a low-temperature ($<850\text{ }^\circ\text{C}$), metal gate NMOS transistor fabrication process that can be found in Refs. 11 and 12. The processing temperature is lowered to satisfy the thermal restriction imposed by the PLZT. A portion of a plasma-enhanced chemical-vapor deposition-grown SiO_2 film, which serves as an ion implantation mask, provides additional support to supplement the van der Waals bonding. For comparison purposes, we have repeated the experiment with a sapphire substrate (instead of PLZT).

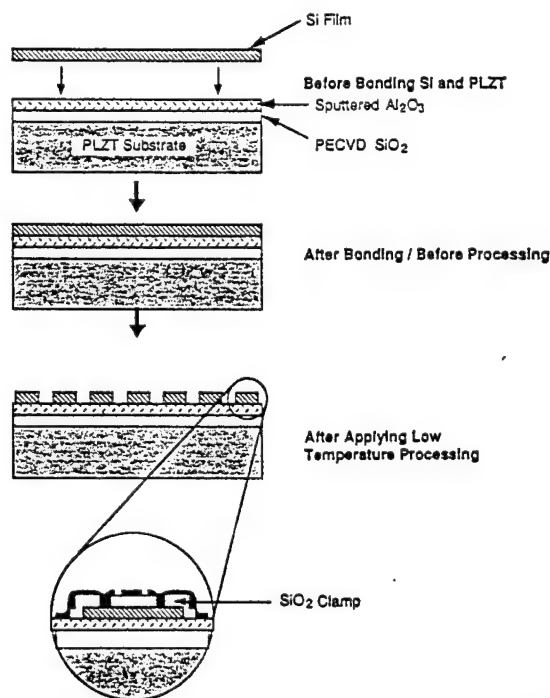


Fig. 2. Schematic illustration of processing steps involved in bonding thin Si wafers to bonded PLZT/sapphire substrates (DB1). A low-temperature processing ($\sim 850\text{ }^\circ\text{C}$ compared with a typical value of $1050\text{ }^\circ\text{C}$) gate oxidation step is applied to fabricate transistor structures on the transferred Si film after bonding. PECVD, plasma-enhanced chemical vapor deposition.

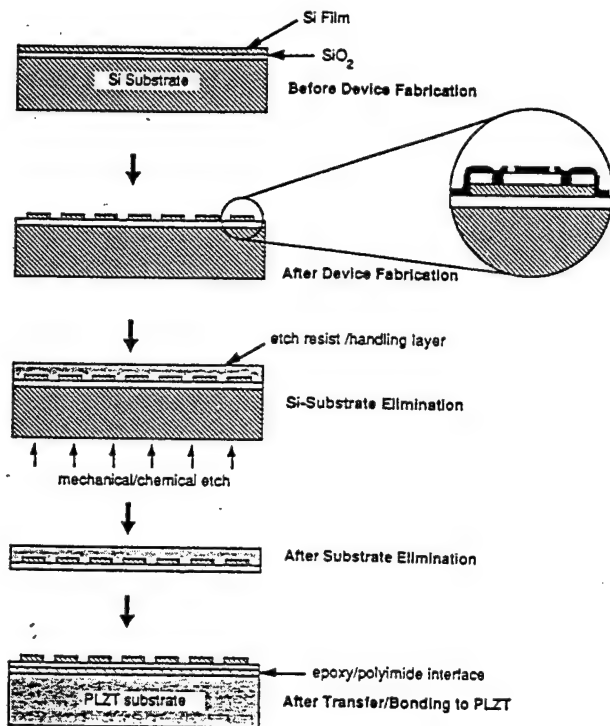


Fig. 3. Schematic illustration of processing steps involved in thinning, transferring, and bonding preprocessed Si device film onto a PLZT substrate (DB2). In this approach, any conventional Si processing step may be applied.

In the second approach (DB2), devices fabricated on the top layer (0.6–1.0- μm -thick Si) of commercially available SOI wafers are lifted off and bonded onto a PLZT substrate. The steps involved in this approach are illustrated in Fig. 3. Mechanical grinding and selective plasma etching are used to remove the host Si substrate of the SOI Si wafer. The resulting film, which consists of isolated Si islands on a SiO₂ layer, is transferred onto a PLZT substrate and is bonded with an adhesion layer of epoxy.¹³ Additional metallization and photolithography are then applied to etch and contact the modulator windows. This approach permits conventional Si processing steps to be applied during device fabrication. The advantage of imposing no limitation on the MOS processing parameters is self-evident.

3. Experimental Results

Owing to the high qualities of Si films, the potential yields of both bonding methods are high. Previously, in collaboration with the Kopin Corporation,¹⁴ we have demonstrated the possibility of transferring and bonding large device areas (up to 30 × 30 mm) that contain 25 transistors/(mm)² with near 100% yield.

Test circuits consisting of metal gate NMOS structures of various gate widths and lengths were fabricated. For comparison, reference samples were fabricated in bulk Si and in the transferred silicon-on-sapphire substrates along with the samples on PLZT

substrates. The electrical performances of NMOS structures on various substrates were compared to evaluate the potentials of direct bonding methods, and are given in Subsections 3.A and 3.B. Changes in threshold voltage V_T , drain-source breakdown voltage V_B , leakage current, and transconductance were measured for this comparison. Subsection 3.C presents the measured performance of transistors (fabricated by the use of the DB2 method) connected in a simple driver circuit configuration.

After the electrical characterization, the performance of the modulators in a fully integrated Si transistor/PLZT structure was measured and compared with a reference modulator structure. The reference structure consisted of a modulator window defined and connected electrically on a polyimide layer (1 μm thick) cured on a PLZT substrate to simulate the Si/PLZT-integrated SLM structure without having the direct bonding steps applied to it. The results are given in Subsection 3.D.

A. Characteristics of N-Channel Metal-Oxide-Semiconductor Transistors Fabricated in Bonded Silicon Film (DB1)

A photomicrograph of NMOS test circuits fabricated on 4- μm -thick Si films (obtained from Virginia Semiconductors) bonded to PLZT with a 20-nm-thick sputtered Al₂O₃ layer as an interface is shown in Fig. 4. The NMOS process included a 850 °C pyrogenic oxidation step. Bonded Si-films withstood this high-temperature step, which affirms the reliability of the bonding. NMOS transistors fabricated in the bonded Si film exhibited electrical characteristics that were comparable with those of similar devices fabricated on bulk Si.¹² The threshold voltages were narrowly distributed between 1.0 and 1.2 V. The drain-source breakdown showed a sharp avalanche behavior, and the breakdown voltages of these transistors were ~25 V and slightly increased with the increasing gate length. The leakage current per unit gate width was 2 pA/ μm following the forming gas sintering. Im-

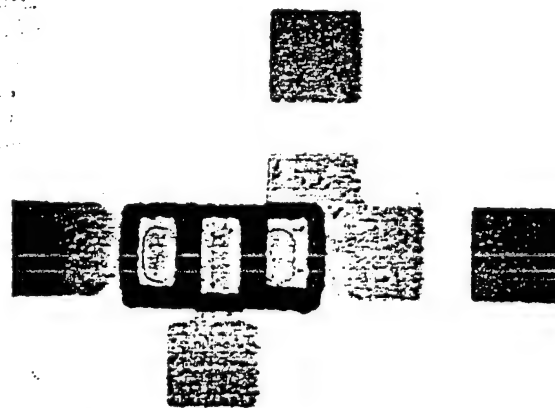


Fig. 4. Photomicrograph of an NMOS transistor fabricated on Si film bonded onto a PLZT substrate with a 20-nm-thick Al₂O₃ buffer layer (DB1).

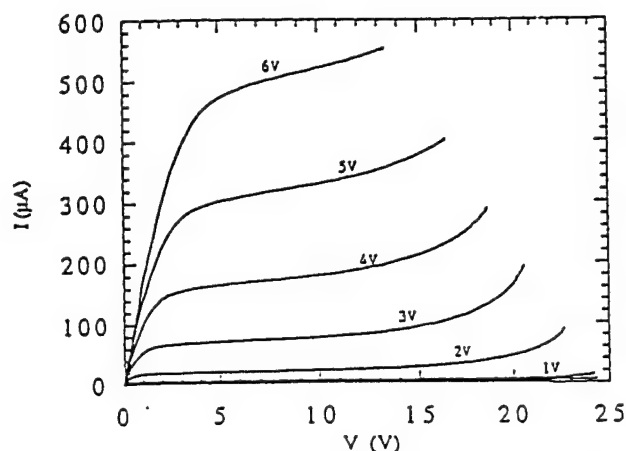


Fig. 5. Typical I-V curves of a $10\text{ }\mu\text{m} \times 20\text{ }\mu\text{m}$ gate NMOS transistor fabricated on bonded Si film (DB1).

proved processing conditions can be expected to lower the leakage current level. Figure 5 represents typical I-V curves of a $10\text{-}\mu\text{m}$ gate length and a $20\text{-}\mu\text{m}$ gate width NMOS transistor. The transconductance of these transistors was approximately $100\text{ }\mu\text{S}$ at $V_{DS} = 10\text{ V}$ for $V_G = 0\text{--}5\text{ V}$ (as indicated by the I-V curves in Fig. 5).

B. Characteristics of Transferred and Bonded N-Channel Metal-Oxide Semiconductor Transistors (DB2)

Utilizing the second approach (DB2), we are now able to routinely etch, transfer, and bond the $10\text{ mm} \times 10\text{ mm}$ Si area that contains NMOS structures onto new substrates. As mentioned above, we have demonstrated the scalability of this method to device areas as large as $30\text{ mm} \times 30\text{ mm}$ in collaboration with the Kopin Corp.¹⁴ To minimize the step height between the PLZT modulator surface and the driving transistor that needed to be connected through a simple metal deposition step [refer to Fig. 6(b)], we used a low-viscosity ($\sim 100\text{ cps}$) optical epoxy that can reduce the adhesive layer thicknesses to less than $2\text{ }\mu\text{m}$.

Photomicrographs of MOS devices before and after etching [Figs. 6(a) and 6(b), respectively] show no discernible degradation in surface quality because of the etch, transfer, and bonding steps. The transferred devices exhibited only a slight change in electrical performance. The I-V curves of NMOS transistors of the same gate size ($W = 10\text{ }\mu\text{m}$ and $L = 20\text{ }\mu\text{m}$) before and after the transfer process are compared in Fig. 7. The threshold voltage of the control sample (remaining on the SOI wafer) was in the range $0.8\text{--}0.9\text{ V}$. Breakdown voltages of both control and transferred samples were $\sim 15\text{ V}$. An $\sim 0.25\text{-V}$ variation in threshold voltage along with a slight increase in transconductance from 39 to $41\text{ }\mu\text{S}$ was observed at $V_{DS} = 10\text{ V}$ and $V_G = 0\text{--}5\text{ V}$ after the transfer. The change in the interface charge at the bonding interface is most likely the cause of the observed variations. The differences in threshold voltage and transconductance between DB1 and DB2 samples can be attributed

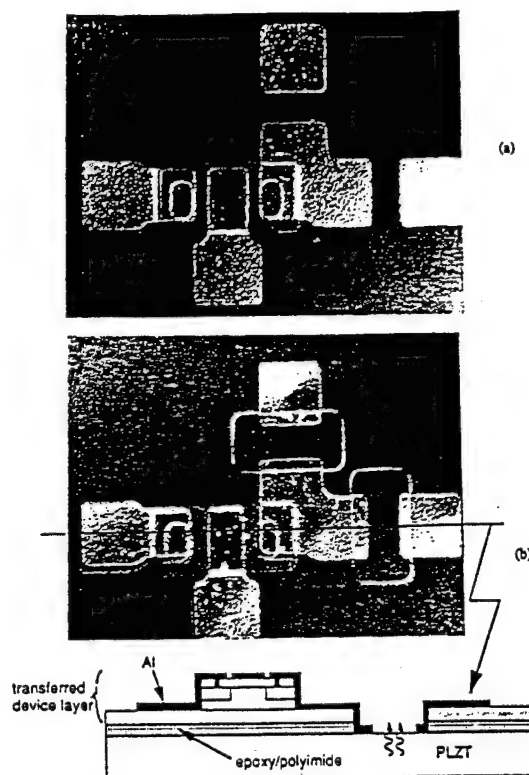


Fig. 6. Photomicrographs of an NMOS transistor (a) on host Si-on-Si substrate before and (b) on PLZT after the etch, transfer, or bond (DB2). A cross section of the bonded structure is also illustrated.

to the difference in the doping concentrations of the substrates used for the two methods.

C. Performance of the Driver Circuit

In order to achieve variable optical modulation, we must connect the modulating medium (PLZT) and the transistors in a circuit configuration similar to that shown in Fig. 8(a). For low supply voltages (e.g., $V_{DD} = 5\text{ V}$), gate sizes for optimal gate

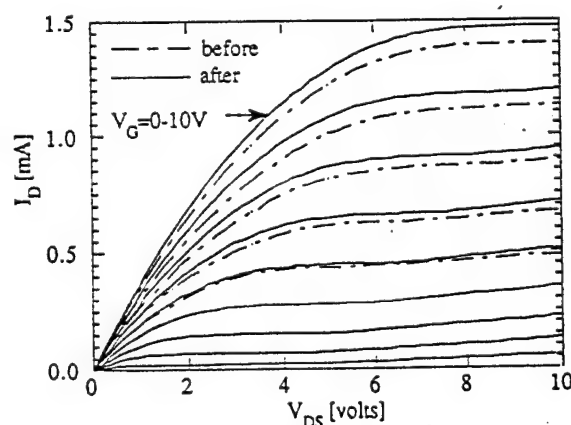


Fig. 7. I-V curves of a transistor with $10\text{-}\mu\text{m}$ -width and $20\text{-}\mu\text{m}$ -length gate size before and after the application of the etch, transfer, and bond steps (DB2).

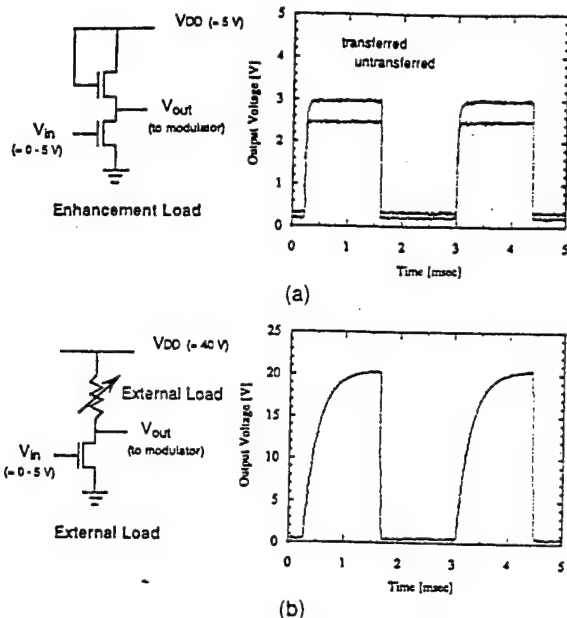


Fig. 8. Inverter connection configurations and typical output traces for 0–5-V square-wave inputs of devices processed with DB2: (a) Actively loaded (enhancement load) inverter. The gate sizes of the corresponding transistors were $L \times W = 20 \mu\text{m} \times 10 \mu\text{m}$ (for load transistor) and $20 \mu\text{m} \times 40 \mu\text{m}$ (for inverting transistor). The output traces are that of a set of these transistors as processed on the SOI wafer (before) and after etch, transfer and bonding (after). (b) Externally loaded inverter. The output trace is that of a $20 \mu\text{m} \times 40 \mu\text{m}$ gate transistor after etch, transfer, and bonding.

width/length ratios between the load and the inverter transistors were available on the test structure. Figure 8(a) shows the inverter configuration and the output voltage curve for a square-wave input. The curve shows a rise time of 20 μ s. For supply voltages (V_{DD}) greater than 10 V, optimal gate size combinations were not available for transistor-loaded inverter connection. Thus the transistors were characterized with external load connections for measurements for which $V_{DD} > 10$ V. The measurement results given in Fig. 8(b) indicate that the maximum output swing is ~ 20 V for $V_{DD} = 40$ V. A further increase in V_{DD} only shifted the same swing slightly up. The breakdown voltage of transistors may be readily improved by modification of the substrate and the process parameters.

D. Performance of a Modulator that is connected to Bonded Silicon Transistor

Modulators that are 30 μm long with 15- μm electrode spacing were characterized after the final metallization step. A photomicrograph of a tested structure is shown in Fig. 6(b). Performances of this structure and a reference modulator structure are presented Figs. 9 and 10. The reference sample consisted of a 1- μm -thick polyimide that was fully cured on a PLZT (9/65/35) substrate with photolithographically defined and contacted modulators identical to those shown in Fig. 6(b). Figure 9(a) shows that at 20 and

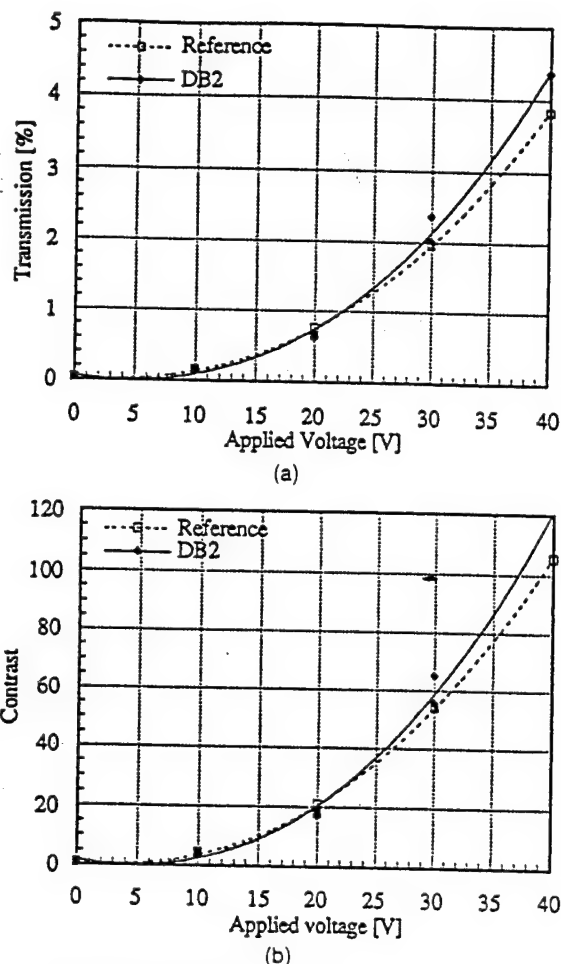


Fig. 9. Performance of modulator that is connected electrically to a transistor on Si film bonded to a PLZT substrate with DB2 compared with that of a reference modulator structure consisting of electrically connected modulator windows of the same size that are photolithographically defined on a PLZT substrate with 1- μm -thick polyimide film. (a) Optical throughput of the modulator shown in Fig. 6(b) versus applied voltage, (b) corresponding contrast ratio versus applied voltage.

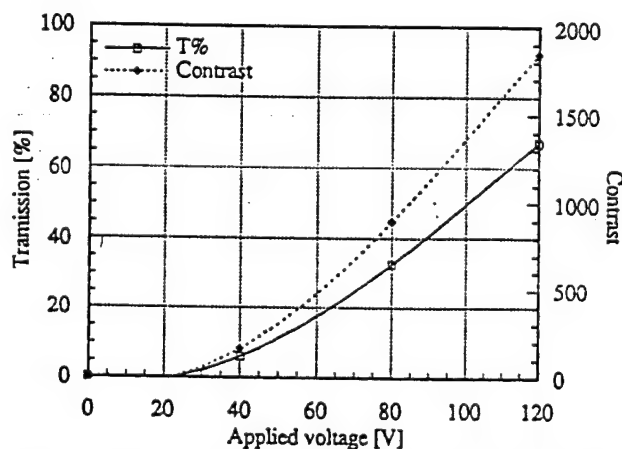


Fig. 10. Throughput and contrast of the modulator shown in Fig. 6(b) as applied voltage is varied in the range 0–120 V.

40 V, transmissions rise to $\sim 0.7\%$ and $\sim 4.5\%$, respectively, from $\sim 0\%$ at $V = 0$; this corresponds to contrasts of 20:1 and 120:1, respectively, as indicated by Fig. 9(b). The results correspond to previously obtained measurement values for modulators of the same size with metal contacts defined directly on PLZT.⁵ When the applied voltage is increased to 120 V, the throughput is increased to $\sim 67\%$ with a corresponding contrast of 1800:1, as shown in Fig. 10. To achieve optimum speed and modulation depth ($\Delta T\%$ for a given ΔV), the modulator may be biased.¹⁵ The abovementioned bonding and NMOS processing steps are demonstrated so as not to degrade the modulator performance as they were all carefully selected and modified to avoid damage to the PLZT substrate.

4. Discussion

A. Selection of Fabrication Method

Both DB1 and DB2 employ near-bulk-quality Si films. Hence logic circuits of any complexity and transistor count can be implemented into the thin Si layer. Method DB1 utilizes thicker ($\sim 4\text{-}\mu\text{m}$) Si films that would readily accommodate the realization of an efficient detector on the film, as mentioned above. However, as all device processing steps are performed after the bonding, this method imposes a rigorous demand on the strength and the quality of the initial Si/PLZT bond. Method DB2 virtually removes this requirement as only two simple lithographic steps (modulator definition and electrical contacting) need to be applied to the structure following the bonding step. As yet, Si layer thicknesses of commercially available SOI wafers ($\leq 1\text{ }\mu\text{m}$) are not sufficient for fabrication of efficient detectors, but DB2 offers the possibility of employing conventional Si technologies for the implementation of circuits of any complexity onto the bonded device layer. Integration of a larger Si area and a PLZT substrate is possible with either method without adding complications to the processing steps.

B. Driver Circuit Simulations

In order to utilize a large array of integrated modulator and driver circuits, as in an S-SLM, each cell in the array should be individually addressable with 5-V signals from a supporting signal processing circuit. However, even the quadratic PLZT modulator requires much larger voltage swings ($\geq 10\text{ V}$) for producing useful light modulation at a typical electrode spacing of $15\text{ }\mu\text{m}$. Thus a large driver circuit output ($> 10\text{ V}$) must be variable with 0–5-V control signal. A modified inverter circuit illustrated in Fig. 11 meets these requirements as a driver circuit. This design was optimized through SPICE numerical circuit simulations. The transient characteristics of this driver are presented in Figs. 12. Figure 12(a) shows a rise time of 100 ns (or a 10-MHz response) for 1-pF modulator load capacitance. Figure 12(b) gives the driver output voltage as the gate voltage on the inverting transistor is varied in the range 0–5 V,

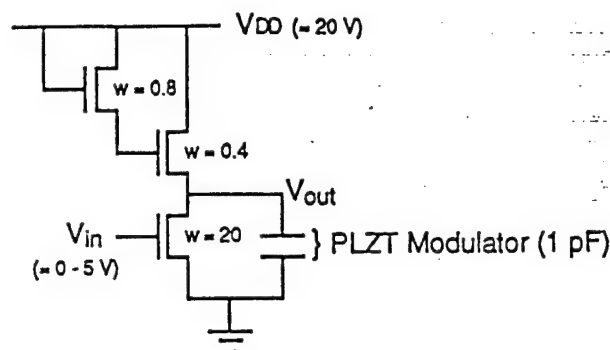


Fig. 11. Schematic illustration of a high-voltage (20-V) inverting circuit for driving PLZT modulators. w (which is width/length) represents the normalized gate widths of NMOS transistors.

demonstrating that the driver output may be used for analog operation.

C. Additional Considerations for Smart Spatial Light Modulator Fabrication

The fabrication of large-array S-SLM's demands other requirements. The addition of demultiplexer, memory cells, and XOR gates required for individually addressable, large-array ($\geq 32 \times 32$) S-SLM's has

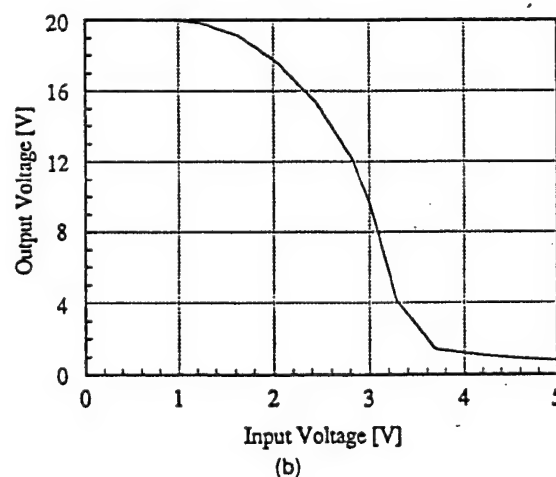
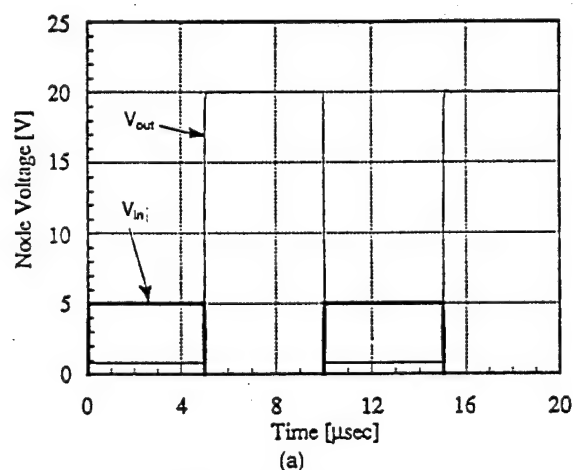


Fig. 12. SPICE simulation for the modulator driver circuit detailed in Fig. 8: (a) transient characteristics for 0–5-V square-wave input, (b) output voltage as a function of 0–5-V input variation.

been considered extensively in the past.⁵ Fabrication methods presented here can readily accommodate these circuit additions. Currently we have completed the design for prototype 8×8 S-SLM's consisting of the discussed driver circuit and 15- μm -aperture PLZT modulators as a step toward producing sophisticated S-SLM's in the near future. After the functionality of an 8×8 S-SLM is demonstrated, further improvement in modulator performance will be desired. The modulator may be dc biased to maximize the modulation of depth without complicating the driver design.¹⁵ The speed of the modulator may be increased by the implementation of a larger driver with more current handling capability.

Conclusion

The successful integration of MOS devices and PLZT substrates for self-contained SLM (consisting of Si driver circuits bonded and connected to PLZT modulators) fabrication by the use of two processing methods was demonstrated. The resulting structures exhibited electrical and optical properties comparable with those of modulator and Si devices fabricated independently in corresponding bulk substrates. The expected performance of a high-voltage ($>20\text{-V}$) driver circuit was also presented. Continued study is under way to combine these technologies to produce high-speed ($>10\text{ MHz}$) S-SLM's with negligible optical absorption for optical computing applications. To add complex processing capability along with better detectors to each S-SLM cell, as shown in Fig. 1, we have also been studying flip-chip bonding with improved alignment accuracy. The results of this research will be presented in a separate paper in the near future. Our objectives are to build both electrically and optically addressable S-SLM's with a direct-bonded driver and addressing circuit and a flip-chip bonded processing circuit. The achievements reported in this paperwork laid the groundwork for a unique type of S-SLM that may offer a new way of overcoming some of the limitations imposed by other optical interconnection technologies for massively parallel optical computing.

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Direct-bonding and Flip-chip Bonding Technologies Applied to Si/PLZT Spatial Light Modulator Fabrication

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Abstract

A versatile technology to graft thin ($\sim 2 \mu\text{m}$ thick) Si circuit layers onto a new host substrate by substrate removal and direct bonding (SR/DB) is presented. This technology has been combined with a self-aligning low-temperature flip-chip bonding technology to fabricate a hybrid Si/PLZT smart spatial light modulator structure consisting of a high voltage driver circuit array, foundry-processed logic chip, and ferroelectric PLZT substrate. Thin Si detectors ($1 \mu\text{m}$ thick) detectors with quantum efficiency of ~ 0.80 has also been implemented in the direct-bonded driver circuit to allow each pixel to be addressed optically. The SR/DB technology can also be applied to bond thin circuit layers onto substrates of any type or shape that may be useful for electronic packaging.

1. Introduction

Establishment of a reliable and cost-effective integration technologies is essential for commercial implementation of high performance electronic and optoelectronic devices. Hybridization allows components of different material systems to be combined to form improved or new devices that cannot be obtained through conventional monolithic integration methods. In particular, the realization of optoelectronic smart pixels needed for high speed parallel input/output functions requires the integration of a light modulating or emitting components, an individually-addressable high voltage ($\geq 15 \text{ V}$) driver circuit array, and a foundry-processed logic chip. To maximize the functionality of such a device, it is necessary to combine material systems and circuit components that are not compatible with each other for monolithic integration. Here, hybridization technologies can be employed to combine the components that are prefabricated separately through conventional methods.

Among possible approaches, *heteroepitaxy* [1,2] and *epitaxial lift-off* (ELO) [3-6] techniques have attracted much attention as means by which integration of Si circuits with GaAs devices can be achieved. In spite of some recent advancements, much work is needed to bring heteroepitaxy to the level of maturity needed for commercial utilization. ELO technology has matured substantially due to a wide-spread effort. It has been applied successfully to transfer and bond, using Van der Waals force, a variety of GaAs-based metal-semiconductor-field-effect transistor (MESFET) [5] and multiple quantum-well (MQW) devices [5,6] onto Si processing chips. However, the reported ELO approaches are often tedious to perform and suffer from scalability and yield problems; such problems prevent them from being adopted for mass quantity production. Moreover, the ELO technique by itself does not promise to result in integrated devices that consist of components of more than two material systems.

To accomplish the task of integrating components of two or more material systems, we have developed techniques to bond a thin Si driver circuit layer onto a ferroelectric lead lanthanum titanate zirconate (PLZT) substrate and flip-chip bond a foundry-processed logic chip to form electrically-addressed and optically-addressed spatial light modulators (E-SLM and O-SLM, respectively). The Si layer bonding process has been applied to transfer and bond large ($2.30 \times 30 \text{ mm}$) device areas and is simple, yet highly reliable. The versatility of this process allows the bonding of prefabricated Si circuit to substrates of any shape and type. As a demonstration, the circuit layer has been bonded to a flexible substrate and shown to be functional under bent conditions. This technology may find a wide range of applications in electronic packaging from smart cards to curved panel displays.

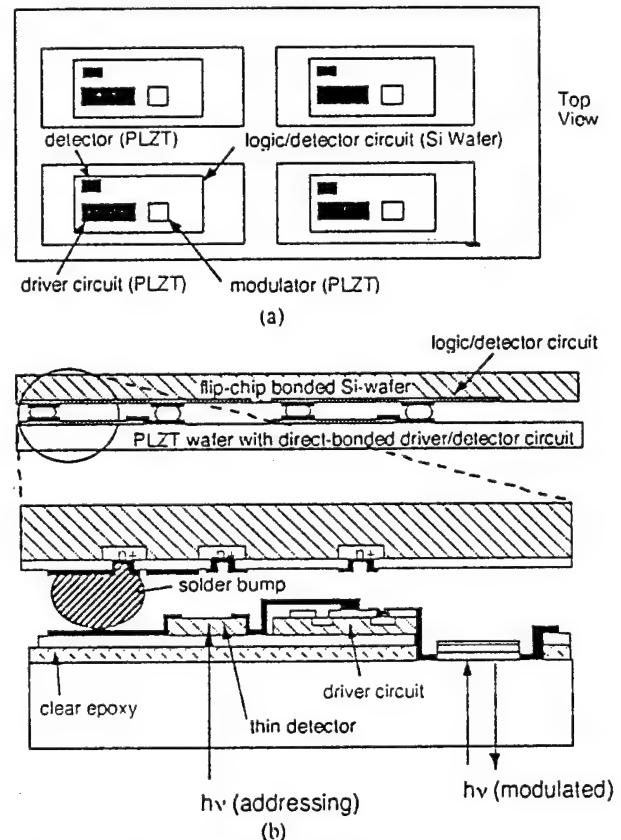


Fig. 1. (a) Top view of a Si/PLZT S-SLM with four cells in a 2×2 array. (b) Cross section of one unit cell of a Si/PLZT S-SLM. A thin Si film with optically addressable driver circuit is direct bonded to a PLZT substrate and flip-chip bonded to a Si wafer with logic and additional detector circuits.

2. Si/PLZT Spatial Light Modulator (SLM) Fabrication

Spatial light modulators (SLM's) are essential for many tasks associated with the development of optoelectronic and optical computing. The SLM's enable the conversion of an array of electrical signals to and from optical signals that are interconnected and propagated more efficiently than electrically interconnected signals. Additional processing capability, or "smarts", can be endowed to individual pixels in the SLM by integrating a foundry-processed logic chip with the SLM; such devices are commonly referred to as smart pixels or smart spatial light modulators (S-SLM's). As single material system cannot be processed to perform both optical and electrical functions associated with SLM's, it is desirable to combine optimal electronic processing materials (e.g., Si and GaAs) and optimal light modulation materials (e.g., ferroelectric ceramics or liquid crystals and III-V semiconductors). Thus, smart pixel structures typically consist of silicon circuits and ferroelectric liquid crystal [7-9], multiple quantum-well (MQW)

[10], or ferroelectric ceramic modulators[11-14]. However, liquid crystal-based smart pixels are too slow, and MQW-based pixels exhibit inherent absorption that limits the light throughput and may cause heat dissipation problem. In order to find a better compromise between speed and light throughput, we have been studying ways to combine silicon electronics with PLZT (a ferroelectric ceramic that do not absorb light) modulators. The operating speeds of Si/PLZT smart pixels are expected to be between those of Si/ferroelectric liquid crystal and MQW devices.

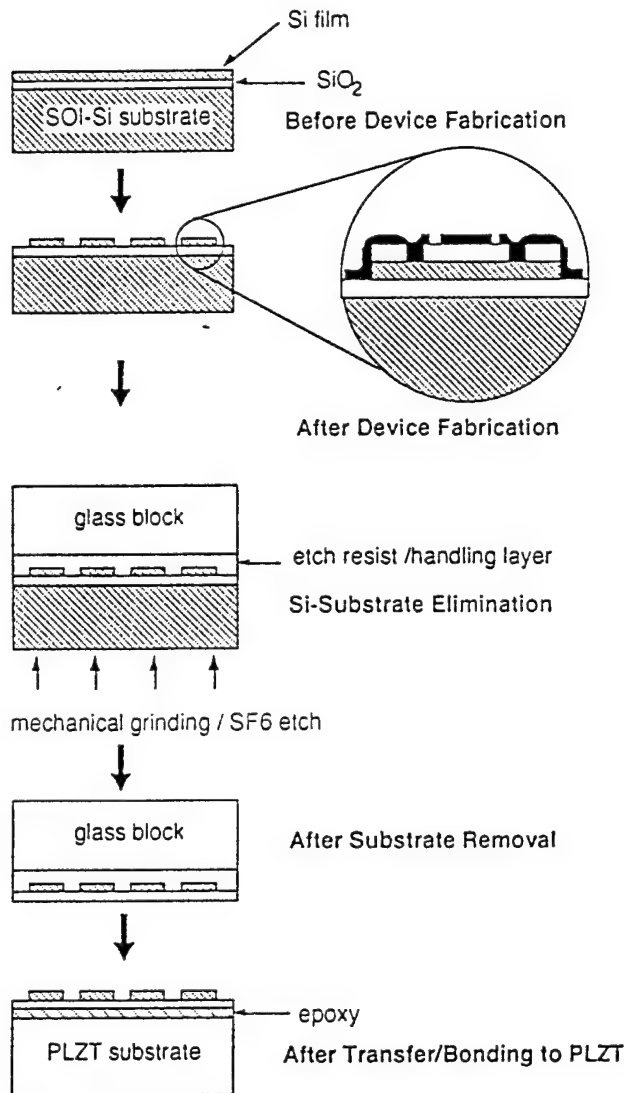


Fig. 2. Substrate removal/ direct bonding processing steps for thinning, transferring, and bonding preprocessed thin Si circuit layer to a PLZT substrate. This process any conventional Si processing steps to be applied to fabricate the circuit layer.

The realization of an Si/PLZT S-SLM requires the integration of an individually addressable array of high voltage silicon driver circuit (requiring ≥ 20 V to operate) with PLZT modulators and a foundry-processed logic chip (operating at 5 V). Schematic illustrations of hybrid Si/PLZT S-SLM's are depicted in Fig. 1. In the depicted structure, a thin film circuit layer (~ 2 μ m thick) containing an array of individually addressable driver circuit (and detector circuit for O-SLM's) is bonded onto a PLZT substrate by applying the SR/DB technology as a first step. A foundry-processed logic chip is then flip-chip bonded to the structure by employing a self-aligning low-temperature flux-less reflow process. By physically separating the high voltage driver circuit from logic circuits, the difficult task of designing and fabricating high and low

voltage circuits on a common chip is avoided.

A. Direct Bonding for Si/PLZT Integration

The integration of bulk quality Si with bulk PLZT was achieved using two methods. In the first method, a commercially available thin (2-4 μ m thick) Si film was Van der Waals bonded to a PLZT substrate with a 200 \AA thick Al_2O_3 buffer layer and sequenced through a low temperature ($\sim 850^\circ\text{C}$) metal gate NMOS transistor fabrication process [13]. Here, the oxidation temperature had to be lowered to stay below the thermal limit of PLZT substrate. Although this approach resulted in devices with acceptable characteristics, the reliability of Van der Waals bonding imposed severe requirements on subsequent processing steps to maintain high yield. Thus, another method, depicted in Fig. 2 was developed to overcome this difficulty. In this second approach (the SR/DB technique) a prefabricated Si circuit layer on an SOI-Si wafer is isolated by eliminating the substrate and bonded onto a PLZT substrate using a thin layer of clear epoxy. Additional photolithography, reactive ion etching, and metallization steps are then applied to connect the bonded Si circuits to the PLZT surface. The yield and scalability of this method is excellent. Grafting and bonding of large device areas (~ 30 mm x 30 mm) has been achieved without requiring additional quality control or processing steps.

In the SR/DB process depicted in Fig. 2, an array of high voltage swing driver circuits, illustrated by the schematic diagram in Fig. 3, is fabricated on a commercially available SOI-Si wafer using conventional NMOS transistor processing steps. The SOI-Si consists a bulk quality thin Si layer (~ 1 μ m thick) which is separated from the bulk Si by a ~ 1 μ m thick layer of SiO_2 . For O-SLM's, p-n⁺ junction detector and amplifier circuit are added to each pixel at the input gate of the driver circuit. Any conventional Si processing steps may be applied to fabricate the thin film circuits as the device layer is grafted onto PLZT after the driver circuit is fully fabricated. A layer of polyimide is applied to the finished circuit to isolate the circuit and metal connections from the second metal layer that is deposited and defined after the circuit is bonded to a new substrate. The SOI-Si wafer is then bonded, using a layer of dissolvable epoxy, onto a clear glass block for subsequent processing and handling. The substrate Si is removed by mechanical and chemical etching. The substrate Si can be thinned to less than 10 ± 2 μ m thickness with relative ease by mechanical grinding alone. The remaining substrate Si is selectively removed by SF_6 plasma etching. The isolated device layer is then bonded to a PLZT substrate with a thin layer of epoxy. For this purpose, droplets of a low viscosity optical epoxy is applied to the PLZT surface and joined with blocked SOI layer. When epoxy droplets are strategically placed over the surface of the PLZT, the surface tension forces of the epoxy spreads the epoxy to form a thin, bubble-free film without additional spreading before the epoxy cures. After the epoxy cured, the handling glass block is removed by immersing the assembly in acetone. Photolithography, reactive ion etching, and metallization steps are then applied to make the final connections between the driver circuit and the modulators.

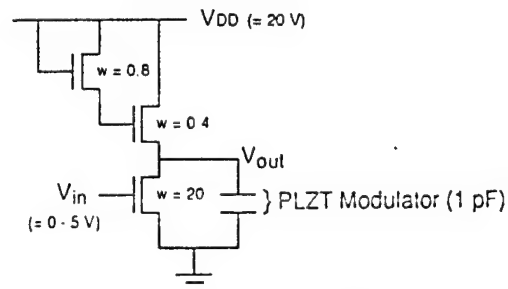


Fig. 3. Schematic illustration of a high voltage-swing (~ 20 V) inverter circuit for driving PLZT modulators. Here, w represents normalized gate widths (width/length) of NMOS transistors. Input can either be an electrical connection or the output from a detector amplifier.

The yield and scalability of this process are excellent. We routinely obtain > 95% overall circuit yield for 15×15 mm areas. Device areas as large as 30×30 mm have been successfully grafted onto a new substrate without further complication, so the scalability of the SR/DB process to wafer-size device area should not be difficult.

Four different Si/PLZT SLM's have been fabricated by using this technology. These include: electrically addressed 8×8 SLM (E-SLM), optically-addressed 5×4 SLM (O-SLM), and two different E-SLM's that are addressed by optically-addressable foundry-processed VLSI network-switching and pattern-matching chips--these chips are flip-chip bonded using the low temperature solder reflow process discussed in Section 2.B. Individual pixels in all four SLM's consist of a variable output (0 - 20 V) driver circuit connected to a $15 \mu\text{m}$ -spaced modulator electrodes ($30 \mu\text{m}$ long). Each pixel in the 8×8 E-SLM's is individually addressed by two-level metal connections that are separated by an insulating layer of polyimide. In O-SLM's, additional detector and amplifying circuit are added to each pixel, as described earlier, and are connected to the input of the driver circuit. The pixels in the E-SLM's for network-switching and pattern-matching VLSI chips are addressed by logic outputs from optically-addressed VLSI chips that are connected to the input gate of the driver circuit via the solder joints.

B. Low Temperature Fluxless Reflow

The network switching and pattern matching smart SLM structures are then completed by flip-chip bonding the corresponding foundry-processed VLSI chips to the E-SLM's following the SR/DB process. As the epoxy used to direct-bond Si/PLZT SLM structure cannot tolerate more than 250°C for a prolonged period of time, it was necessary to develop a low temperature controlled-collapse-chip-connection (C4) reflow process. To accomplish this task, a ball-limiting pad metallurgy (BLM) that allows the use of near-eutectic Sn/Pb solder alloy was designed and fabricated. Here, Cr/Cr-Cu/Cu BLM layers are sputtered onto the connection pads on the direct-bonded Si/PLZT E-SLM's through a mask. Sn/Pb (60/40) alloy solder bumps ($50 \mu\text{m}$ dia. and $25 \mu\text{m}$ thick) are then electroplated on top of the pads. Bonding pads on the foundry-processed logic chips are defined by electroless plating of Ni/Au (0.5 and $0.2 \mu\text{m}$ thick, respectively). The described metallurgy also can be utilized to achieve self-alignment of the bonding pads by exploiting the surface tension forces of the solder during the reflow [15]. A designed experiment confirmed that initially misaligned chips can be self-aligned to better than $2 \mu\text{m}$ accuracy with the described pad geometry. A detailed photomicrograph in Fig. 4, shows the features of a fully assembled pattern-matching logic chip that is flip-chip bonded, using the described self-aligning C4 bonding technology, to a matching Si/PLZT SLM.

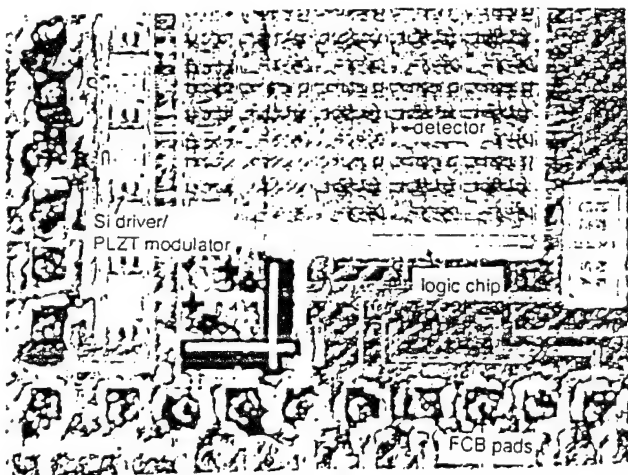
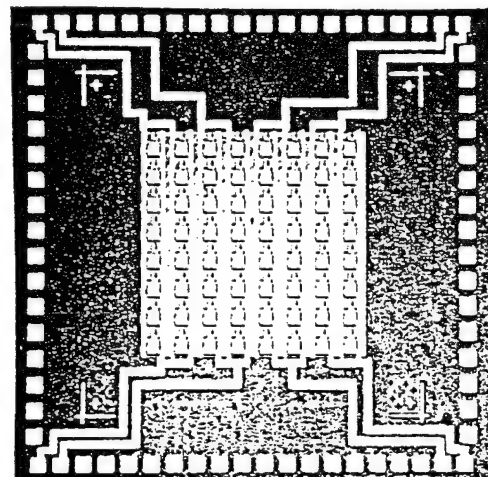


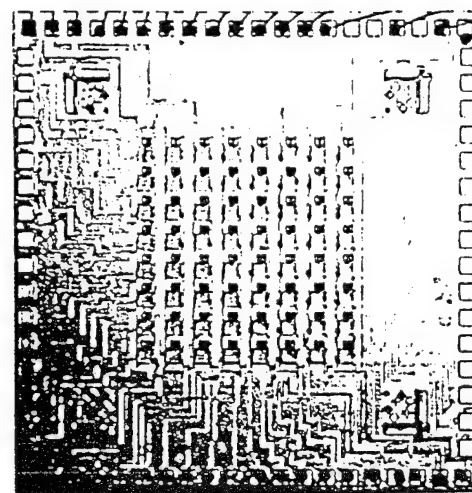
Fig. 4. A photomicrograph of a fully assembled pattern matching S-SLM that consists of direct-bonded Si/PLZT SLM's that are addressed by a flip-chip bonded optically addressable logic chip.

C. Experimental Results

The E-SLM, O-SLM, and S-SLM's exhibit no degradation in device performance. Photomicrographs of an 8×8 driver circuit array before (on SOI-Si wafer after device processing) and after bonding to PLZT substrate using the described SR/DB process is shown in Figs. 5(a) and 5(b), respectively. The photomicrographs show no degradation in surface quality of the devices before and after the application of SR/DB process. We find that this observation consistently translates to no degradation in device performance, as presented in the following sections.



(a)



4.0 mm
(b)

Fig. 5. Photomicrographs of an 8×8 driver circuit array (a) after MOS processing (before substrate removal) and (b) after substrate removal, direct bonding to a PLZT substrate, and second metal layer deposition and definition steps.

C.1 Direct-bonded Driver and Detector Circuit Performance

In a previous work, we demonstrated that SR/DB process does not degrade the performance of MOS transistors [14]. The output characteristics of a driver circuit direct-bonded to a PLZT substrate, depicted in Fig. 6, promise up to 10 MHz operation for 1 pF modulator load; breakdown voltage of this was ~ 25 V. The output characteristics of the optically-addressed SLM is shown in Fig. 7. Here, the pixel was addressed by a diode laser ($\lambda=830$ nm) beam that is pulsed with a TTL signal. The breakdown voltage of reference optically-addressed driver circuit processed in bulk was

measured to be ~ 15 V. It should be noted that integrated detectors are only ~ 1 μm thick. Section 3.A discusses the expected performance of these thin detectors in more detail.

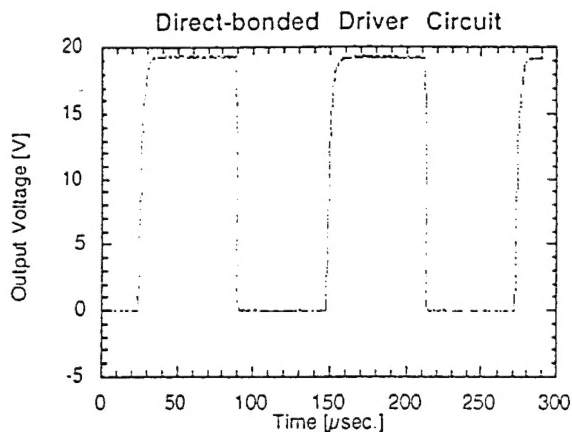


Fig. 6. Oscilloscope trace of a direct-bonded 20 V driver circuit, illustrated in Fig. 3, for a 20 pF load. Rise time is ~ 5 μs . Breakdown voltage was ~ 25 V.

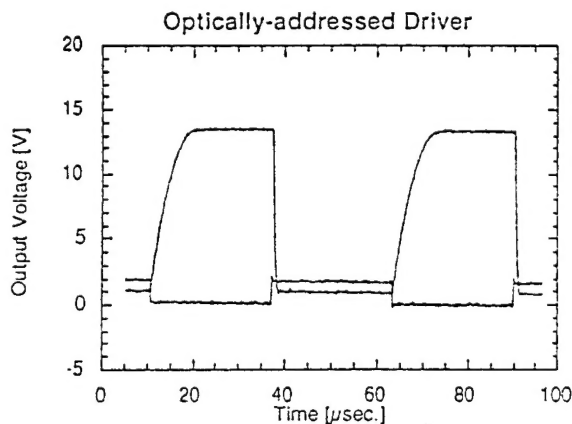


Fig. 7. Oscilloscope trace of an optically addressed direct-bonded 20 V driver circuit. Rise time is ~ 12.3 μs for a 15 pF load. Breakdown voltage was ~ 15 V.

C.2 Modulator and Smart Pixel Performance

In the same work referenced in the previous section, we demonstrated that modulator performance is not changed by the SR/DB process; better than 20:1 output contrast with the integrated driver circuit is observed. This is not surprising since the PLZT substrate is never exposed to a processing condition that could reduce its electrooptic properties. The functionality of a pixel in a network switching S-SLM is illustrated in Fig. 8. In this S-SLM, the optical signal from a pulsed diode laser is detected by four input detectors of the logic chip. The detected signals are sequentially processed by the logic chip and queued to an output buffer that is connected to the input of the modulator driver of the Si/PLZT SLM. The modulator in turn modulates the incident CW laser beam (He-Ne) according to this input signal, and the output signal from the modulator is detected by an external detector which is connected to an oscilloscope.

3. Applications of Direct Bonding Technology

The versatility of SR/DB process allows the integration of thin Si devices onto virtually all types of surfaces; the substrate surfaces may be curved or flexible. In addition, semi-transparency of thin (1 –

2 μm thick) Si device layers may be utilized to obtain unique optoelectronic devices. Thus, in the following sections, we present preliminary study results that examine the characteristics of thin Si detector and issues related to the applications of SR/DB.

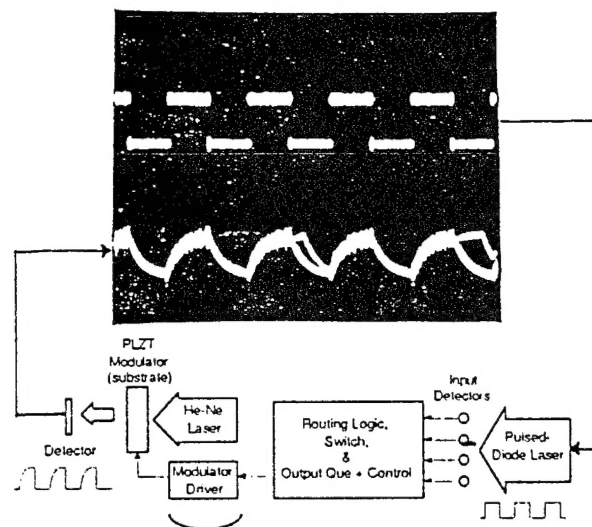


Fig. 8. Oscilloscope trace of detected signal at the output of SLM pixel driven by an optically-addressed network-switching logic chip.

A. Semi-transparent Si Detector

The functionality of thin Si detectors and amplifying circuits was discussed briefly in Section 2.C.1. To study their characteristics more thoroughly, p-n⁺ junction detectors were fabricated in bulk Si and commercially available SOI-Si wafers with two different Si layer thicknesses— 1 μm SOI-Si from Kopin Corp. and 3 μm SOI-Si from SEH Corp. Thin detectors formed on SOI-Si are semi-transparent due to their thinness. Normalized optical transmission curves of Si as a function of thickness for different wavelengths are plotted in Fig. 9; reflection losses are taken into account. This plot shows that 1 μm thick detectors absorb only about 30% of the incident light at $\lambda=633$ nm. Thus, thin detector and amplifier circuit can be utilized as a passive sensor that can transmit 70% or more of the incident light signal.

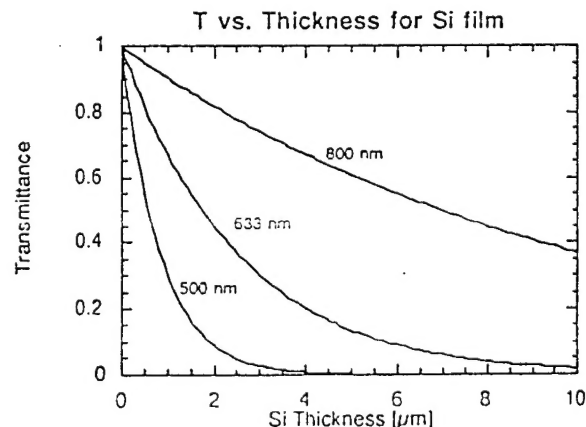


Fig. 9. Normalized optical transmission curves of Si films as a function of thickness for three different wavelengths.

The effective quantum efficiencies (as measured) of 1 μm thick Si detectors are ~ 0.24 at $\lambda=633$ nm; this gives normalized quantum

efficiency (compensated for finite absorption of ~ 0.30 at $\lambda=633$ nm for a $1\text{ }\mu\text{m}$ thick Si detector) of about .80. Bulk Si detectors have quantum efficiencies of about 0.82 at this wavelength. Thus, thin Si detectors exhibit bulk-like characteristics. Output current from $1\text{ }\mu\text{m}$ and $3\text{ }\mu\text{m}$ thick detectors are compared to that of bulk detectors for various incident optical powers in Fig. 10. The plot indicates that normalized characteristic of detectors formed in $1\text{ }\mu\text{m}$ thick Si is virtually same as that of detectors formed in $3\text{ }\mu\text{m}$ thick SOI-Si. It also should be noted that $3\text{ }\mu\text{m}$ thick detector performance is close to that of bulk detectors since it absorbs more than 70% of the incident light at $\lambda=633$ nm, as indicated by Fig. 9. Fig. 10 also shows that SR/DB process does not degrade the performance of thin detectors. Slight improvement, apparent in the graph, may be due to the increase in electron mobility as the residual interfacial stress between Si and SiO_2 layers is partially relaxed during the SR/DB process. Output voltages from the amplifier circuits integrated with 1 and $3\text{ }\mu\text{m}$ thick detectors (see Fig. 11) show that even $1\text{ }\mu\text{m}$ thick detectors may be utilized for analog optical addressing. These results suggest that for S-SLM's, detector circuits may be integrated with the driver circuit in the direct-bonded thin Si layer to liberate more area on the foundry-processed chip for additional logic circuits.

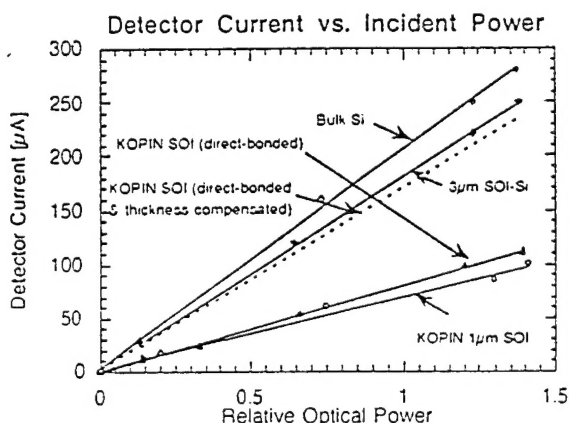


Fig. 10. Detector current as a function of incident optical power for bulk, 1 and $3\text{ }\mu\text{m}$ thick detectors. Note that substrate removal/direct bonding process does not degrade the thin ($1\text{ }\mu\text{m}$ thick) detector performance.

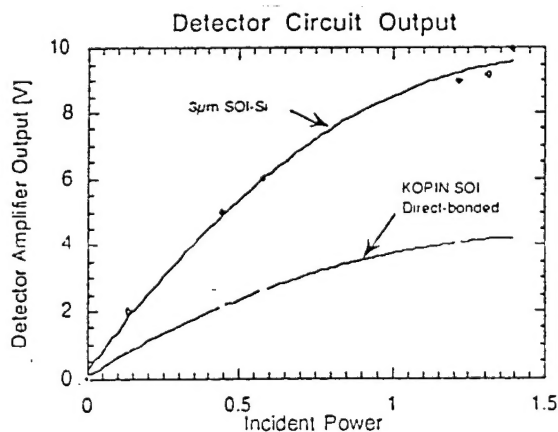


Fig. 11. Detector amplifier output as a function of incident optical power for 1 and $3\text{ }\mu\text{m}$ thick detectors. The plot suggests that these detectors may be addressed by an analog optical signal.

B. Flexible Circuit

Owing to the thinness of initial SOI layer on Si substrate, which is typically $\sim 2\text{ }\mu\text{m}$ thick, the isolated SOI layer is quite flexible after substrate removal. By inserting an additional flexible handling layer between the handling block and the SOI sample, the device layer can be bonded onto surfaces of almost any contour. We successfully transferred a 20 V driver array (used for E-SLM's) onto a flexible substrate to characterize the influence of bending on the electrical performance of the driver circuit. The same circuit was measured before and after wrapping the flexible circuit around a 1 cm dia. test tube as shown in Fig. 12. The output characteristics, shown in Fig. 13, indicate that the applied amount of bending had no influence on the performance of the circuit when compared to the performance of an untransferred reference array in SOI-Si.

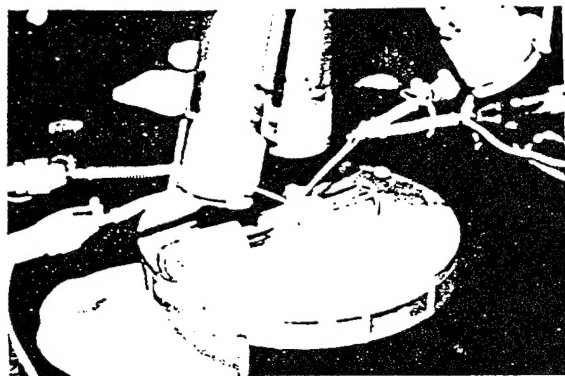


Fig. 12. A photomicrograph of a flexible circuit wrapped around a 0.5 cm radius test tube in a test set-up.

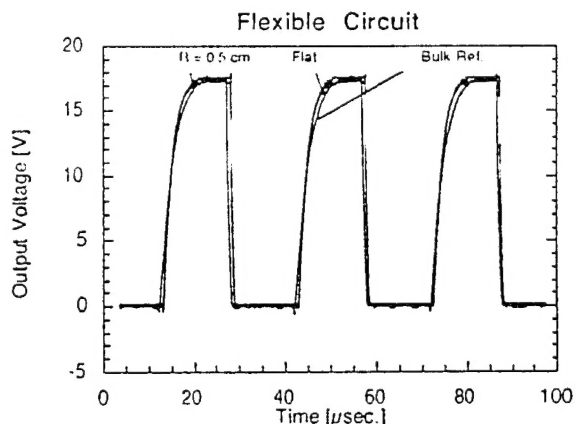


Fig. 13. Transient performance comparison of flat and bent ($r = 0.5\text{ cm}$) 20 V inverter (driver) circuit compared to a reference circuit fabricated in bulk Si. The trace indicates that bending had no effect on the circuit performance.

The maximum amount of strain ϵ_n that can be applied to a brittle ceramic before it suffers permanent fracture can be approximated by

$$\epsilon_n = \frac{K_c}{E} \frac{1}{\sqrt{\pi a}} \quad \text{Eq (1)}$$

where K_c is fracture toughness, E is the Young's modulus, and a is the maximum crack size [16]. For Si and SiO_2 , K_c is about $0.8 - 1.0\text{ MNm}^{-3/2}$, and Young's modulus are 107 and 94 GNm^{-2} , respectively. This leads to strain limits of 0.06 and 0.006 for 10 nm and $1.0\text{ }\mu\text{m}$ crack sizes, respectively. However, these values are still greater than the "rule of thumb" maximum strain for ceramics of ~ 0.001 (0.1%). The maximum strain on a Si film bent to radius R can be determined from a simple geometric argument, by assuming that lattice spacing on the concave side of a bent Si film is not changed. The strain on the outer surface of the film can then be

be approximated by

$$\epsilon_n = \frac{t}{R} \quad \text{Eq. (2)}$$

where t is the film thickness and R is the radius of curvature of the bent film. For a 1 μm thick Si film, the "rule of thumb" maximum strain of 0.1% gives a minimum radius of curvature of about 1 mm. This bending limit was tested on several free-standing Si films: 2-4 μm thick Si films obtained from Virginia Wafer Inc. and 1 μm thick Si film layers isolated from SOI-Si wafers from Kopin Corp. We were indeed able to bend these films repeatedly to less than 1 mm radius without fracturing the film. A similar test was performed on an isolated Si/SiO₂ layer without etching away the SiO₂ preferentially in buffer HF. The Si/SiO₂ layer rolled up to ~1 mm radius due to the relaxation of residual stress between the two layers, but it was possible to unroll and bend the film the other way to about 1 mm radius repeatedly without fracturing the film.

According to Eq. (1), the maximum strain on the lattice is only 0.02% for bending radius of 0.5 cm. The electron mobility μ is inversely proportional to the effective electron mass m which is roughly proportional to the inverse square of the lattice spacing [17]. Thus, with effective carrier mass m approximated by

$$m = m_0 \frac{E_g}{2(h^2 / m_0^2 \chi \pi / a)^2 + E_g} \quad \text{Eq. (3)}$$

for conduction band carrier with band gap energy E_g and lattice spacing a , the change in mobility μ can be related to the change in lattice spacing (that is, the strain ϵ_n) by the approximations,

$$\begin{aligned} \mu &\propto \frac{1}{m} \propto \frac{1}{a^2} \\ \Rightarrow \Delta\mu &\propto \frac{2\Delta a}{a^3} = \frac{2}{a^2} \epsilon_n \\ &\Rightarrow \frac{\Delta\mu}{\mu} \propto 2\epsilon_n. \end{aligned} \quad \text{Eq. (4)}$$

Eq. (4) suggests that even at 0.1% strain limit for Si, the mobility of electron is changed by less than 0.2%. As a comparison, a study by Zhang and Tsien report that residual interfacial stress in zone-melt recrystallized SOI (ZMR-SOI similar to SOI-Si wafer available from Kopin Corp.) is sufficient to cause 17.2% change in electron mobility [17]. Thus, the application potential of physically flexible, complex Si circuit layer is promising.

C. Discussion and Potential Applications

Due to the inherent thinness, the detectors fabricated in SOI can operate at higher frequency than those fabricated in bulk Si--due to reduced capacitance and diffusion lengths. Thin Si detector structures that can operate at 100 GHz has been reported [18]. Such detector structure promises direct integration of high speed (> 1 GHz) Si detector and pre-amplifier circuits to Si for reduced production cost.

In order to optimize the described technologies for industrial utilization, further experiments and analysis need to be performed to analyze the structures of direct-bonded and flexible circuits from a material science point of view. Since fracture strengths of epoxies are typically less than that of SiO₂, fractures will begin in the epoxy layers. This is normally not a problem for rigid substrates, but for flexible substrates, it can lead to premature fracture-failure of thin device layers. Thus, alternative adhesives that are highly elastic yet strong need to be identified. The tribology of the interfacial structure consisting of a thin device layer, adhesive, and substrate need to be studied extensively to identify the failure mechanism in order to enhance the flexibility and strength of the thin device layers.

Flexible circuit technology can be utilized to fabricate numerous devices and systems that cannot be realized with conventional technology. This technology can be employed to fabricate contoured CCD, detector, or sensor arrays for applications ranging from wide

angle video-imaging to medical sensors. It can also be applied to produce flexible smart cards. The circuits bonded to a light-weight flexible substrate will also be resilient to mechanical shocks. Recent developments in the area of semiconducting polymer transistor technology drew much attention due to its potential toward making rollable circuits [19]. However, this technology can only provide devices with electronic properties far inferior to Si and requires a substantial amount of material development effort. The flexible thin film Si circuit technology already offers many of the advantages that polymer transistor technology promises to offer in the future at a far greater level of maturity.

The requirement of SOI-Si wafer imposes certain limitations on the applicability of SR/DB and flexible circuit technologies. Although, due to the large added VLSI processing expense, the cost of initial substrate is a small fraction of the processed wafer, the SOI-Si wafers are fairly expensive compared to bulk Si, and special arrangements need to be made to apply foundry services to these wafers. Thus, there is a need to explore the possibility of obtaining thin flexible circuit layers directly from processed bulk Si wafers. When Si wafers are thinned to ~10 μm or less through mechanical grinding, they begin to transmit some light. By monitoring the intensity distribution of the transmitted light, thin Si can be lapped further to less than 1 μm thickness uniformly across the sample area. The equations describing the flexibility of thin Si films (Eqs. (1) & (2)) indicate that fracture size need to be minimized in order to maximize the fracture strength of the films. Thus, we are currently investigating simple ways to obtain surface smoothing and thinning of final few microns of mechanically thinned Si wafer. Results of preliminary experimentations with chemo-polishing techniques--to obtain and preferentially remove porous Si layers on Si without employing anodic chemical etching [20-21]--are promising.

Finally, four types of SLM's fabricated by SR/DB and flip-chip-bonding need to be characterized further. The functionality of these devices need to be assessed by implementing them in various optoelectronic system configurations. Moreover, other modulator or emitter candidates need to be considered for integration with Si. VCSEL's are promising as emitters that can be integrated with Si circuit. Recently reported developments in electroluminescent porous Si diodes also merit some attention as they may be directly integrated onto grafted Si layers [22].

4. Conclusion

A substrate removal and direct bonding technology by which thin (~2 μm thick) Si circuit layers can be obtained and bonded to a new host substrate has been combined with a self-aligning low-temperature flip-chip bonding technology to fabricate four different hybrid Si/PLZT SLM and S-SLM structures consisting of high voltage driver circuit array, foundry-processed logic chip, and ferroelectric PLZT substrate. The electrical and optical performances of components in the hybrid structures were not significantly different from that of separately fabricated bulk-reference samples. Optically-addressed SLM's consisting of semi-transparent thin detectors were found to be functional. Inherent flexibility of isolated device layer has been exploited to bond devices onto curved and flexible substrates. We observed no discernible change in the performance of thin flexible Si circuits under various bending conditions. Experiments indicate that 1 μm thick Si layers can be bent to less than 1 mm radius repeatedly without fracturing. Flexible circuit technology lends itself to a wide range of electronic packaging opportunities from smart cards to flexible display panels and conformal packaging.

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